



# AKAI

## SERVICE MANUAL





Model: LCT42Z5TAP

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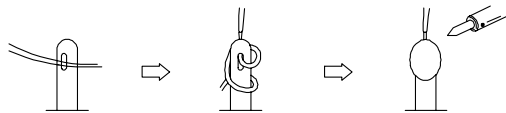
.....  
This manual is the latest at the time of printing, and does not  
include the modification which may be made after the printing,  
by the constant improvement of product.  
.....

# Safety Precaution

 <div style="border: 1px solid black; padding: 5px; text-align: center;"><b>CAUTION</b> <b>RISK OF ELECTRIC SHOCK</b> <b>DO NOT OPEN</b></div>  <p><b>CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT REMOVE COVER (OR BACK). NO USER-SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL ONLY.</b></p>	 <p>The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated "dangerous voltage" within the product's enclosure that may be of sufficient magnitude to constitute a risk of electric shock to persons.</p>  <p>The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.</p>
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## PRECAUTIONS DURING SERVICING

- In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements.  
Examples: RF converters, tuner units, antenna selection switches, RF cables, noise-blocking capacitors, noise-blocking filters, etc.
- Use specified internal Wiring. Note especially:
  - Wires covered with PVC tubing
  - Double insulated wires
  - High voltage leads
- Use specified insulating materials for hazardous live parts. Note especially:
  - Insulating Tape
  - PVC tubing
  - Spacers (insulating barriers)
  - Insulating sheets for transistors
  - Plastic screws for fixing micro switches
- When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



- Make sure that wires do not contact heat generating parts (heat sinks, oxide metal film resistors, fusible resistors, etc.)
- Check if replaced wires do not contact sharply edged or pointed parts.
- Make sure that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

## MAKE YOUR CONTRIBUTION TO PROTECT THE ENVIRONMENT

Used batteries with the ISO symbol



for recycling as well as small accumulators (rechargeable batteries), mini-batteries (cells) and starter batteries should not be thrown into the garbage can.

Please leave them at an appropriate depot.

### WARNING:

Before servicing this TV receiver, read the **SAFETY INSTRUCTION** and **PRODUCT SAFETY NOTICE**.

## SAFETY INSTRUCTION

The service should not be attempted by anyone unfamiliar with the necessary instructions on this apparatus. The following are the necessary instructions to be observed before servicing.

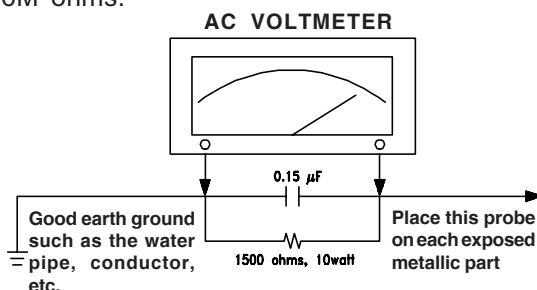
- An isolation transformer should be connected in the power line between the receiver and the AC line when a service is performed on the primary of the converter transformer of the set.
- Comply with all caution and safety related provided on the back of the cabinet, inside the cabinet, on the chassis or picture tube.
- To avoid a shock hazard, always discharge the picture tube's anode to the chassis ground before removing the anode cap.
- Completely discharge the high potential voltage of the picture tube before handling. The picture tube is a vacuum and if broken, the glass will explode.

5. When replacing a MAIN PCB in the cabinet, always be certain that all protective are installed properly such as control knobs, adjustment covers or shields, barriers, isolation resistor networks etc.
6. When servicing is required, observe the original lead dressing. Extra precaution should be given to assure correct lead dressing in the high voltage area.
7. Keep wires away from high voltage or high temperature components.
8. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads, metal overlay, control shafts, etc., to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly to the AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5K ohms volt sensitivity or more in the following manner. Connect a 1.5K ohm 10 watt resistor paralleled by a 0.15 $\mu$ F AC type capacitor, between a good earth ground (water pipe, conductor etc.,) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination of the 1.5K ohm resistor and 0.15  $\mu$ F capacitor. Reverse the AC plug at the AC outlet and repeat the AC voltage measurements for each exposed metallic part.

The measured voltage must not exceed 0.3V RMS.

This corresponds to 0.5mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.

The resistance measurement should be done between accessible exposed metal parts and power cord plug prongs with the power switch "ON". The resistance should be more than 6M ohms.



**AC Leakage Current Check**

## PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in this apparatus have special safety-related characteristics.

These characteristics are often passed unnoticed by visual inspection and the protection afforded by them cannot necessarily be obtained by using replacement components rated for a higher voltage, wattage, etc.

The replacement parts which have these special safety characteristics are identified by  $\triangle$  marks on the schematic diagram and on the parts list.

Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire, or other hazards.

9. Must be sure that the ground wire of the AC inlet is connected with the ground of the apparatus properly.

## 1 Do not power on

### 1.1 Please check the AC cable if connect to AC plug.

It is true that the connector doesn't connect to AC plug. Please connect it.

### 1.2 Please check the AC cable if connect to AC power.

It is true that the AC cable doesn't connect to AC power. Please connect it.

### 1.3 Please check the power board of fuse if broken.

If the F1 fuse is broken, firstly please pull out the AC cable from AC power. Secondly please check whether the AC L power and the AC N ground have shortened, the multimeter read number is infinite, and the fuse is broken. Then look over power board if the Output whether is normal. Please change the power board.

## 2 The LED (indicator light) is extinguished

### 2.1 The LED (indicator light) is green or red; to put the power switch when the indicator light is worked. It is true that the Power DC Output have somewhere short circuit.

Please check the connector J2, J1. If not, please connect the direction whether is wrong, or the main board somewhere of power short circuit.

## 3 The power is normal worked, but doesn't show screen

### 3.1 The indicator light worked normal (green light).

Please check the main board of transistor Q2 whether right, if not, doesn't have +5V voltage.

It is true Q2 Collector hasn't +5V, to check Q2 if fail. Or to check Q2 of base if not low (low is working, high doesn't working).

Please refer to the attached sheet a circuit diagram.

### 3.2 Please check the backlight of connector if the direction or the connector of wire computer direction is wrong.

### 3.3 To check the connector panel of voltage is +24V, it's true. Then to check the first pin if it has +5V voltage, it's true, than to check the power board of +24V voltage, it's true, and the panel of backlight board is fail. To change the panel of backlight board.

Please refer to the attached datasheet.

## 4 The screen doesn't have picture but backlight.

### 4.1 To check the panel of voltage, and the main board of bead R342 connect if not ok. Then check the R342 of voltage is +12V(27 inch panel voltage is +5V, and to check R338). The connector J9 if isn't +12V(27 inch panel voltage is +5V). Please to check the power board of connector CON5 if has +12V(27 inch panel voltage is +5V)

### 4.2 To check the main board +12V voltage. Then to check the main board QF3 of the first pin if +12V voltage, if fail. It's low (close 0v) working.

Please refer to attached sheet a circuit diagram.

## 5 The remote control doesn't be control.

### 5.1 To check the batteries of remote control if it runs out of.

### 5.2 To check the main board of connector J3 of wire connects fastness and the connector if broken.

Please refer to the attached sheet a circuit diagram.

## 6 The sound doesn't output

### 6.1 To check the main board +24V voltage of connector J2, it's not +24V voltage. Then to check the power main board +24V.

Please refer to the attached sheet a circuit diagram

## 7 Picture abnormality

Please change the LCD model panel when the picture displays horizontal or vertical level line or flash spots.

## Product Specification

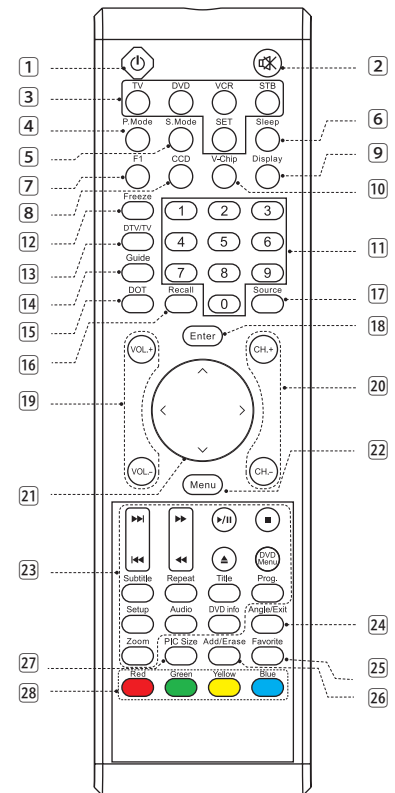
Product Model	LCT42Z5TAP
TV System	NTSC M, ATSC
VIDEO System	NTSC
Screen Size	42" diagonal
Active Area	930.24mm (W) x 523.26mm(V)
Aspect Ratio	16:9
External Size (with stand)	1067.3mm (W) x 781.2mm (H) x 275mm (D)
Gross Weight	34 kg
Display Resolution	1366 (H) x 768 (V) pixels (Each pixel has R/G/B 3 color cells)
Display Color	16.7 millions of colors (R/G/B each 256 scales)
Gray Scale	256 (R/G/B each 8-bit)
Brightness (Peak Value)	500cd/m <sup>2</sup>
Contrast (Dark Room)	800:1
Sound Effect	Acoustic Cinema Enhancement
Power Supply	AC 120V~, 60 Hz
Power Consumption	300W
Input Terminal	Antenna Input (F Type) x 1 (NTSC + ATSC/Clear QAM)
	HDMI (Ver. 1.2) connector x2
	VGA (D-Sub 15 Pin Type) x 1
	Component Video - YPbPr x 2 RCA Terminals
	Video Input RCA Terminal x 1
	S-Video Input Mini Din 4 Pin Terminal x 1
	Stereo, Audio x 5
Output Terminal	1 set of Audio Output terminals (RCA, L&R)
	SPDIF (Coaxial for all) x 1

*Note: The specifications shown above may be changed without notice for quality improvement.*

## Remote Control

(Note: Details refer to AKAI TV Universal Remote Control Programming Guide.)

- 1 **Standby**(⏻): Press to turn on and off.
- 2 **Mute**(⏸): Press this button to quiet the sound. Press again to reactivate the sound.
- 3 Press these buttons to select control of the TV, DVD, VCR or Set-top Box device.
- 4 **P. Mode**: Press to cycle through the picture modes: Cinema, Normal, Vivid, Hi-Bright and User.
- 5 **S. Mode**: Press to cycle through the sound modes: Normal, News, Cinema, Concert and User.
- 6 **Sleep**: Press repeatedly until it displays the time in minutes (10, 20, 30, 40, 50, 60, 90, 120 and Off) that you want the TV to remain on before shutting off. To cancel sleep time, press **Sleep** button repeatedly until sleep Off appears.
- 7 **F1**: Press to cycle through the Stereo and Multi-channel TV sound options: Mono, Bilingual and Stereo.
- 8 **CCD**: Press to select the Closed Caption mode.
- 9 **Display**: Press to display the channel information; this information disappears after 9 seconds.
- 10 **V-Chip**: Select the child protect mode you want.
- 11 **0~9 Number Buttons**: Press 0~9 to select a channel, and input the password.
- 12 This button is not for controlling the television.
- 13 **DTV/TV**: Press to choose DTV/TV (high definition channels) directly.
- 14 **Guide (Digital TV Timetable)**: Press to display the (Digital TV Timetable) mode. Press again to exit.
- 15 **DOT**: Press number buttons with it to select the channels directly in DTV. (i.e. channel 108-1 would need the dot button after the 8)
- 16 **Recall**: Press to return to previous channel. (Only for TV)
- 17 **Source**: Press to display the input source menu. There are TV, AV, S-Video, YPbPr 1, YPbPr 2, VGA, HDMI 1 or HDMI 2. If you are selecting inputs from the input menu or displaying the OSD menu, press the **Enter** button to confirm your selection.
- 18 **Enter**: Press to enter or confirm.
- 19 **VOL +/-**: Press to adjust the audio levels.
- 20 **CH +/-** : Press to select the channel forward or backward.
- 21 **^, v, <, >**: Press **^**, **v**, **<**, **>** to move the on-screen cursor.
- 22 **Menu**: Press to enter into the on-screen setup menu, press again to exit.
- 23 These buttons are not for controlling the television.
- 24 **Exit**: Press this button to exit in the menu.
- 25 **Favorite**: Press to display favorite channel list, press **^** or **v** select channel then press **Enter** button to confirm.
- 26 **Add/Erase**: Press to add or delete favorite channels.
- 27 **Pic Size**: Press to change the screen size, such as Full, 4:3. (Note: When in VGA mode, it can only select "Full".)
- 28 **Color Button**:
  - Red**: This is a special control function for the Digital tuner.
  - Green**: This is a special control function for the Digital tuner.
  - Blue**: This is a special control function for the Digital tuner.
  - Yellow**: This is a special control function for the Digital tuner.



## Support the Signal Mode

### A. VGA Mode

Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
640 x 480	31.50	60.00
800 x 600	35.16	56.25
	37.90	60.32
	48.08	72.19
1024 x 768	48.40	60.00

### B. YPbPr Mode

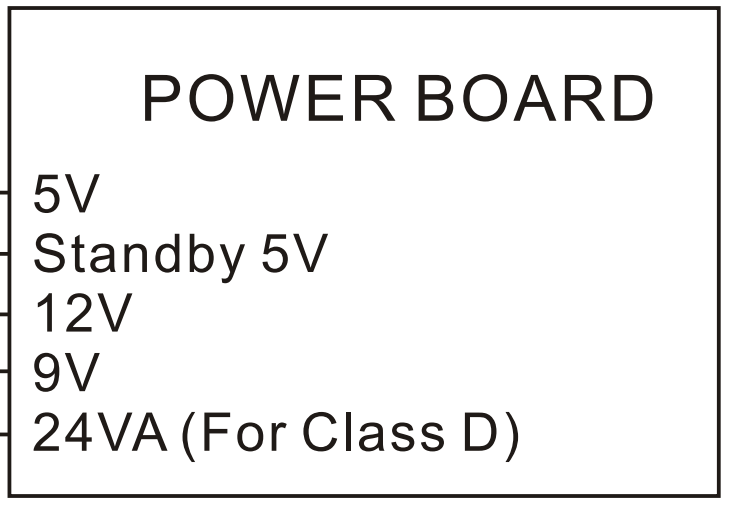
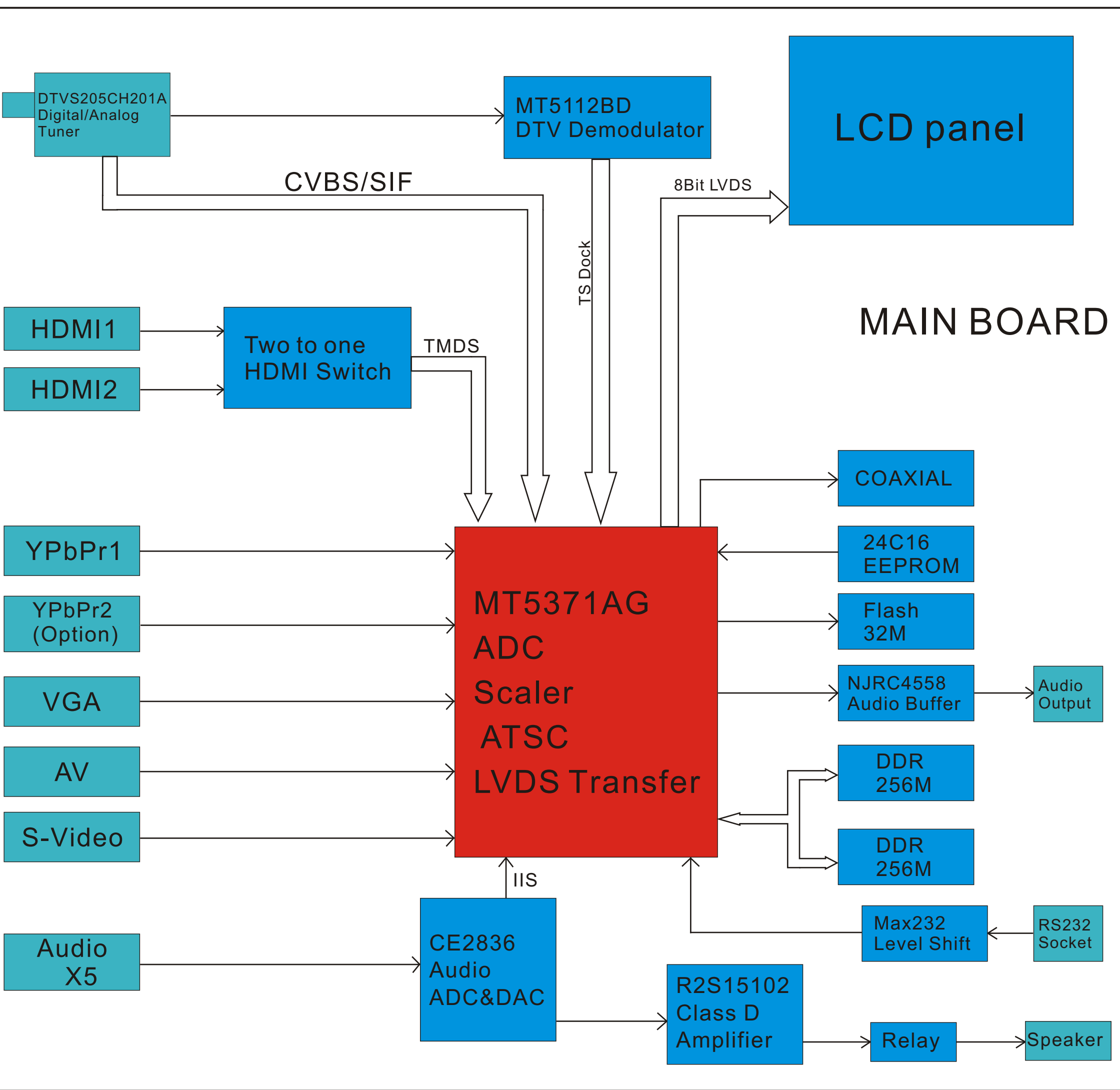
Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
480p(720x480)	31.468	59.94
720p(1280x720)	45.00	60.00
1080i(1920x1080)	33.75	60.00

### C. HDMI Mode

Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
480p	31.468	59.94
720p	45.00	60.00
1080i	33.75	60.00

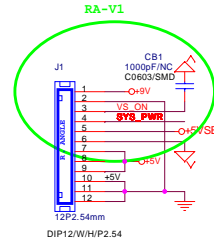
- When the signal received by the Display exceeds the allowed range, a warning message shall appear on the screen.
- You can confirm the input signal format from the on-screen.



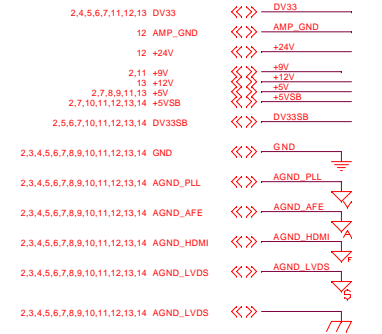
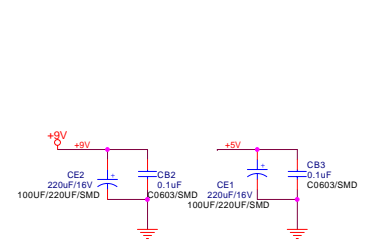


# MT5372RAV6 MT5372 (PBGA) REFERENCE DESIGN - 4 LAYERS

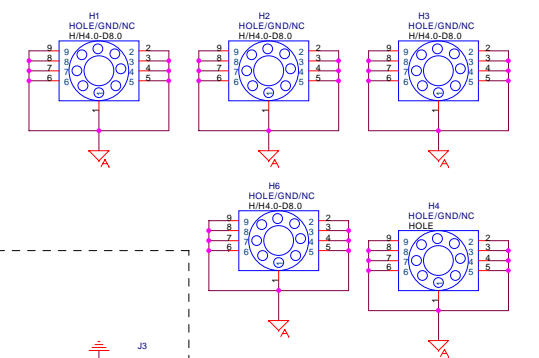
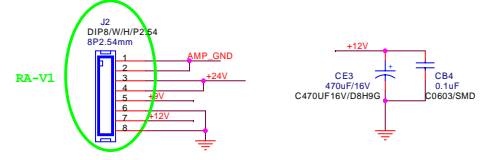
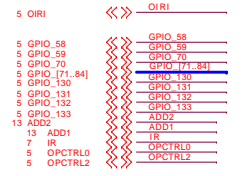
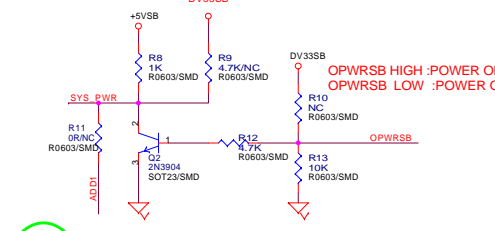
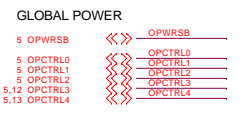
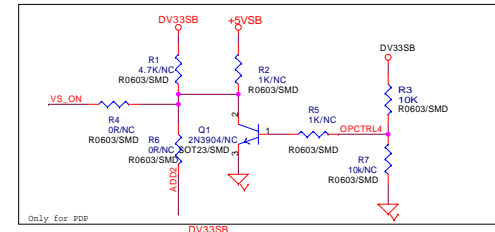
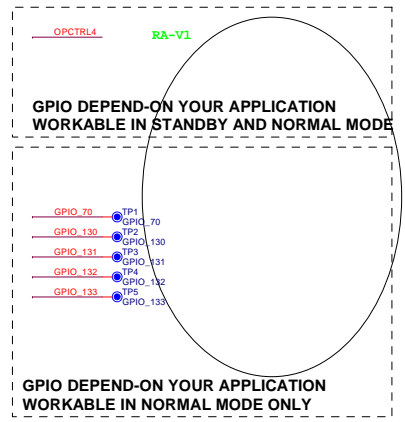
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RA-V0	INITIAL VERSION	2006/07/14
RA-V1		2006/07/31
RA-V2		



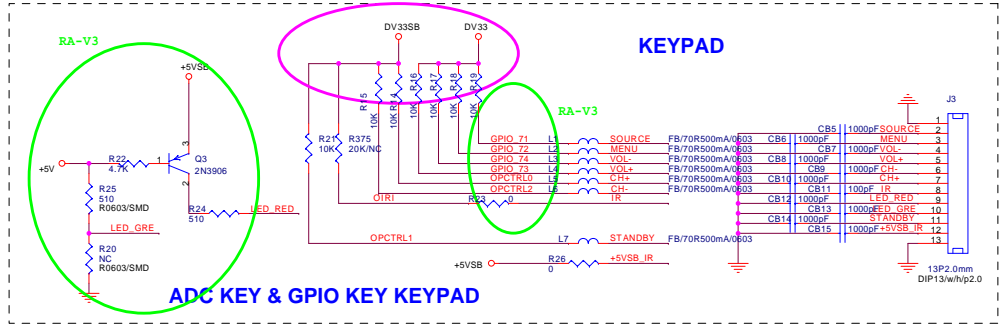
## POWER INPUT



01. INDEX
02. POWER
03. TUNER
04. MT5112 ASIC
05. MT5372 ASIC
06. MT5372 BYPASS CAP.
07. MT5372 PERIPHERAL
08. DDR1 MEMORY
09. YBPBR INPUT
10. HDMI/VGA INPUT
11. AUDIO CODEC
12. AUDIO AMP



NAME	TYPE	DEVICE
+24V	POWER +24V	POWER SUPPLY
+12V	POWER +12V	POWER SUPPLY
+5V	POWER +5V	POWER SUPPLY
+5VSB	POWER +5V	POWER SUPPLY
DV33SB	POWER +3.3V	STANDBY POWER
+5V_TUENR	POWER +5V	TUNER POWER
DV33_DM	POWER +3.3V	MT5112 POWER AND ITS PERIPHERAL
DV18_DM	POWER +1.6V	MT5112 POWER
DV33	POWER +3.3V	MT5372 POWER AND ITS PERIPHERAL
AV33	POWER +3.3V	MT5372 ANALOG POWER
DV18_DDR	POWER +1.8V	MT5372 DDR POWER
AV15	POWER +1.5V	MT5372 VIDEO FRONT-END POWER
DV12	POWER +1.2V	MT5372 POWER
AV12	POWER +1.2V	MT5372 ANALOG POWER
GND	GROUND	DIGITAL GROUND
AGND_PLL	GROUND	ANALOG GROUND
AGND_AFE	GROUND	ANALOG GROUND
AGND_HDMI	GROUND	ANALOG GROUND
AGND_LVDS	GROUND	ANALOG GROUND



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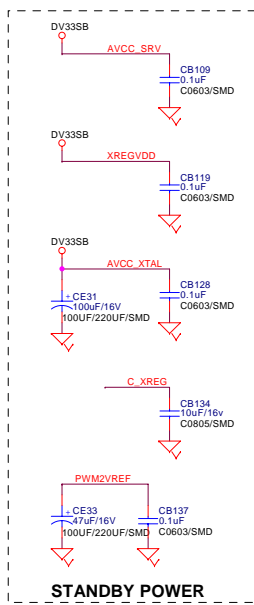
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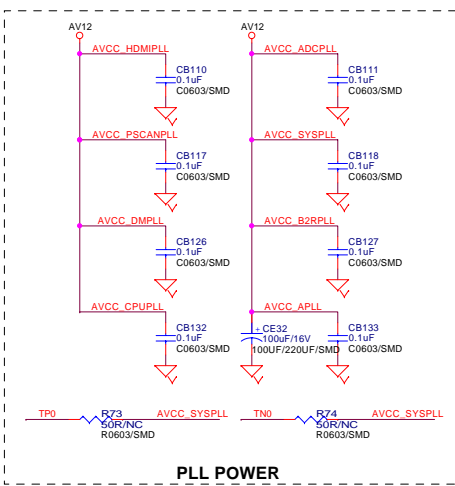




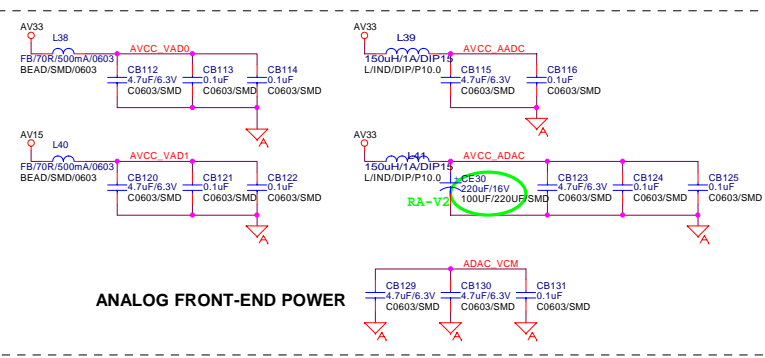




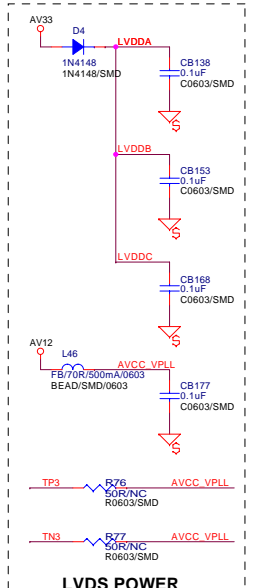
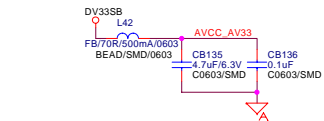
**STANDBY POWER**



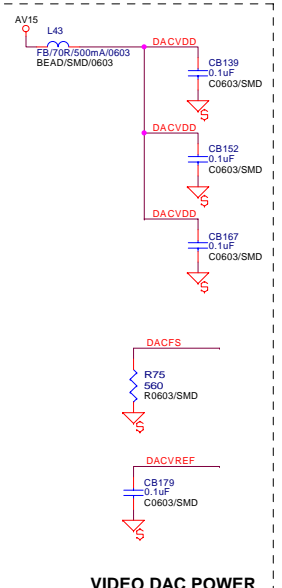
**PLL POWER**



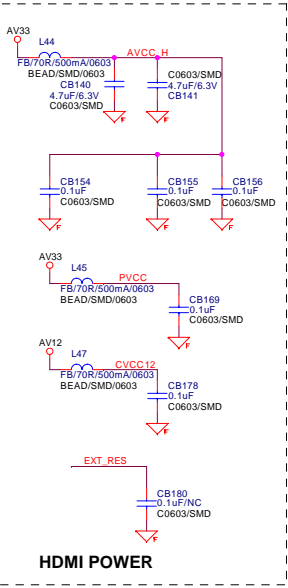
**ANALOG FRONT-END POWER**



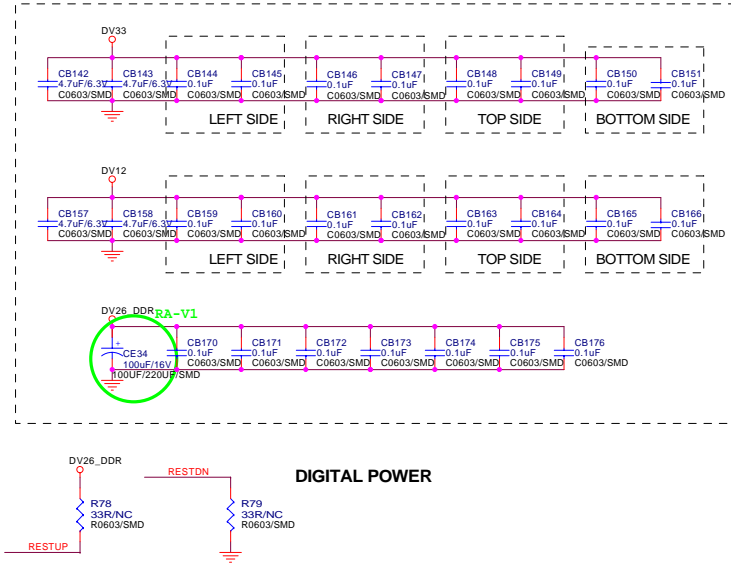
**LVDS POWER**



**VIDEO DAC POWER**

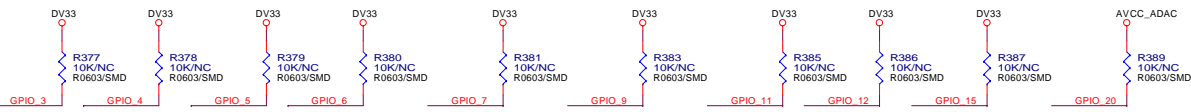


**HDMI POWER**



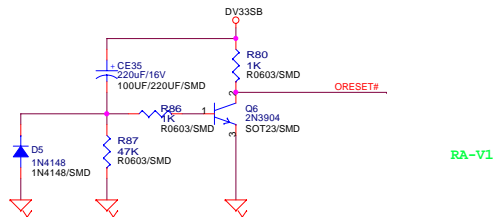
**DIGITAL POWER**

1,2,4,5,7,11,12,13	DV33	AVCC_H	AVCC_H
2,10,11,14	AV33	PVCC	PVCC
2,4,8	DV26_DDR	CVCC12	CVCC12
2,5	AV15	EXT_RES	EXT_RES
2,5	AV12	AGND_HDMI	AGND_HDMI
1,2,3,4,5,7,8,9,10,11,12,13,14	DV33SB	AGND_LVDS	AGND_LVDS
	GND	DACVDD	DACVDD
		DACVREF	DACVREF
		AGND_LVDS	AGND_LVDS
		AVCC_SRV	AVCC_SRV
		XREGVDD	XREGVDD
		AVCC_XTAL	AVCC_XTAL
		C_XREG	C_XREG
		PWM2VREF	PWM2VREF
		RESTUP	RESTUP
		RESTDN	RESTDN
		DV12	DV12
		DV33SB	DV33SB
5,12	GPIO_10	GPIO_3	GPIO_3
5,13	AVCC_ADAC	GPIO_4	GPIO_4
		GPIO_5	GPIO_5
		GPIO_6	GPIO_6
		GPIO_7	GPIO_7
		GPIO_8	GPIO_8
		GPIO_9	GPIO_9
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		GPIO_15	GPIO_15
		GPIO_16	GPIO_16
		GPIO_20	GPIO_20

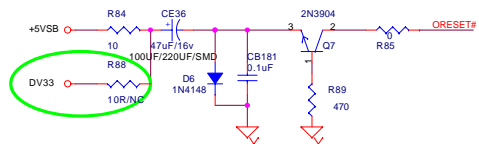


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 Custom: Checked: <Checker> Sheet: 6 of 14  
 Date: Friday, December 29, 2006

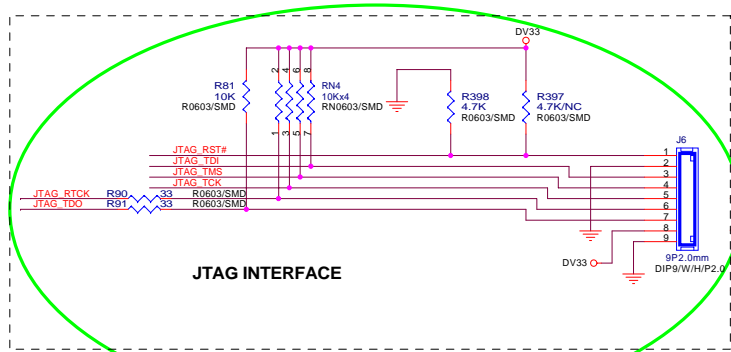
**POWER ON RESET# CIRCUIT**



**POWER DOWN RESET# CIRCUIT**



RA-V1



**JTAG INTERFACE**

RA-V2

1,2,8,9,11,13	+5V	<<>>	+5V
1,2,10,11,12,13,14	+5VSB	<<>>	+5VSB
1,2,4,5,6,11,12,13	DV33	<<>>	DV33
1,2,5,6,10,11,12,13,14	DV33SB	<<>>	DV33SB
3,4,5,6,8,9,10,11,12,13,14	GND	<<>>	GND
3,4,5,6,8,9,10,11,12,13,14	AGND_PLL	<<>>	AGND_PLL
2,3,4,5,6,8,9,10,11,12,13,14	AGND_AFE	<<>>	AGND_AFE

5	ORESET#	<<>>	ORESET#
5	OXTALI	<<>>	OXTALI
5	OPWMO	<<>>	OPWMO
7	POOE0#	<<>>	POOE0#
8	POOE0W	<<>>	POOE0W
8	POWER#	<<>>	POWER#
5	PDDI[0..7]	<<>>	PDDI[0..7]
6	PDA[0..22]	<<>>	PDA[0..22]

**NOR FLASH**

5	JTAG_RST#	<<>>	JTAG_RST#
5	JTAG_TDI	<<>>	JTAG_TDI
5	JTAG_TMS	<<>>	JTAG_TMS
6	JTAG_TCK	<<>>	JTAG_TCK
5	JTAG_RTCK	<<>>	JTAG_RTCK
5	JTAG_TDO	<<>>	JTAG_TDO

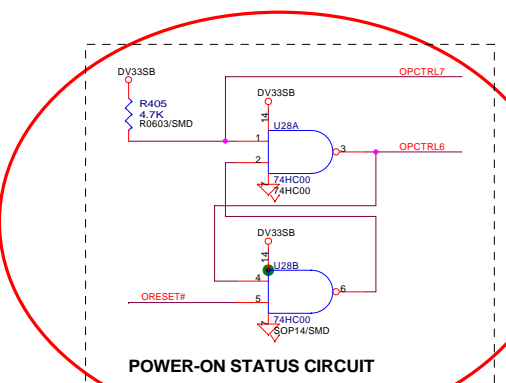
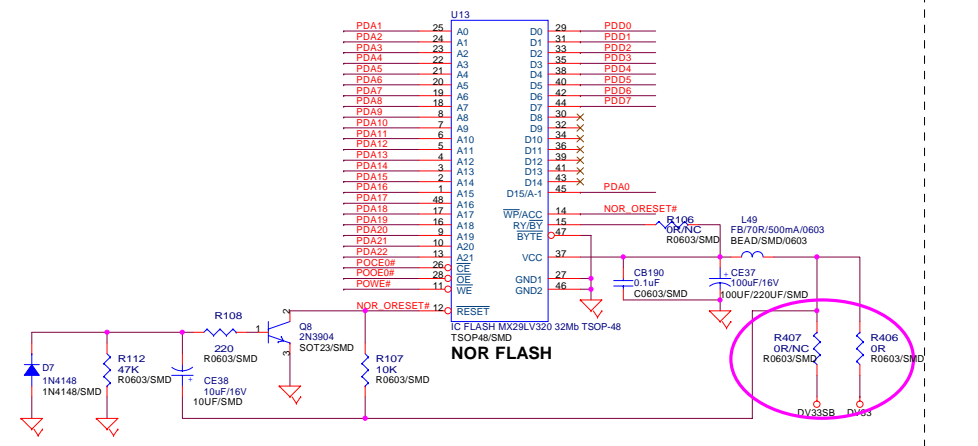
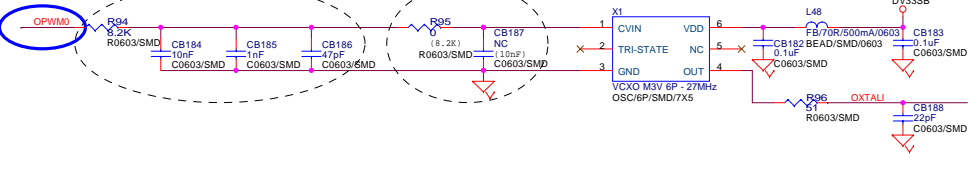
**JTAG**

5	OPCTRL6	<<>>	OPCTRL6
5	OPCTRL7	<<>>	OPCTRL7
5	SMCE#	<<>>	SMCE#
5	DCLK	<<>>	DCLK
5	MCLK	<<>>	MCLK

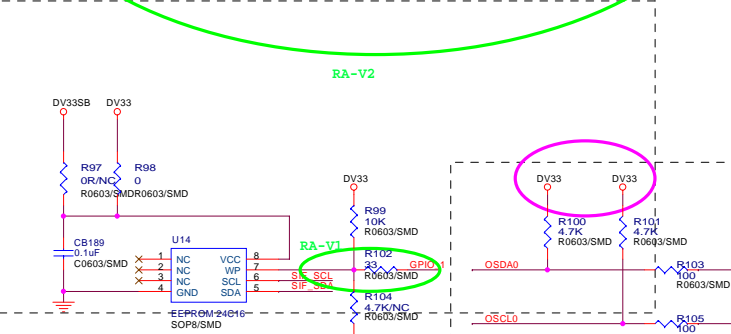
5,13	OSDA0	<<>>	OSDA0
5,13	OSCL0	<<>>	OSCL0
4,11	SIF_SDA	<<>>	SIF_SDA
4,11	SIF_SCL	<<>>	SIF_SCL

4,5	GPIO_0	<<>>	GPIO_0
5	GPIO_1	<<>>	GPIO_1
5,6	GPIO_11	<<>>	GPIO_11
5,6	GPIO_12	<<>>	GPIO_12
5,6	GPIO_15	<<>>	GPIO_15
5,6	GPIO_16	<<>>	GPIO_16
5,13	GPIO_16	<<>>	GPIO_16
5	GPIO_17	<<>>	GPIO_17

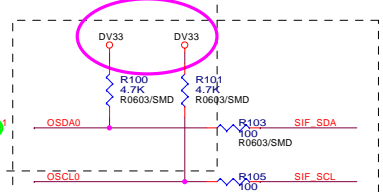
9	DVD_IR	<<>>	DVD_IR
1	IR	<<>>	IR



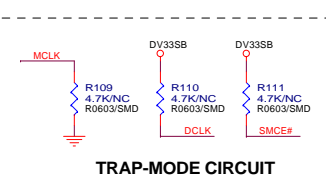
RA-V3



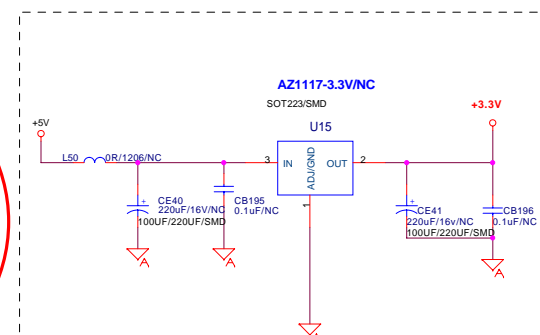
**MT5372 SYSTEM EEPROM**



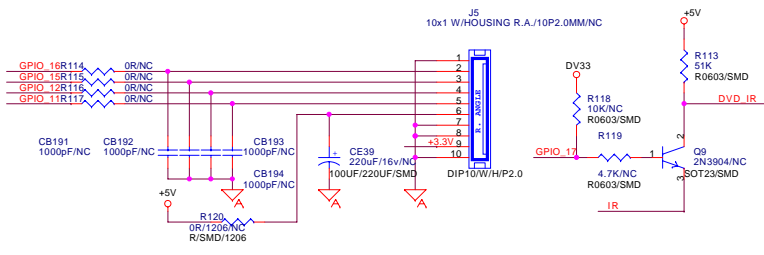
**GENERAL PURPOSE SIF**



**TRAP-MODE CIRCUIT**



**DVD POWER CONTROL**



**ZhongShan KAWA Electronic Inc.**

Part: **MT5372 PERIPHERAL**

Document Number: **MT5371\_V07**

Design: <Designer> Rev: 2

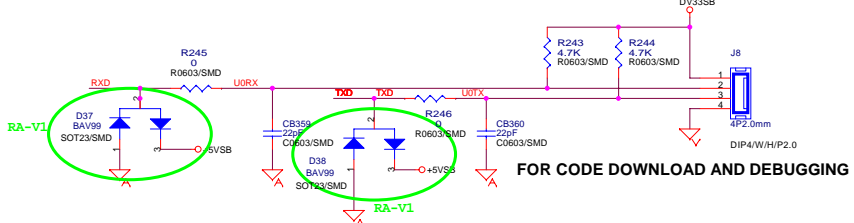
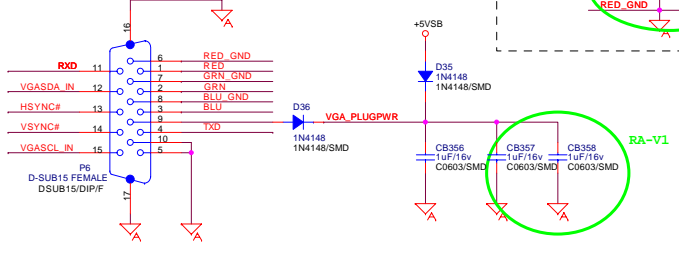
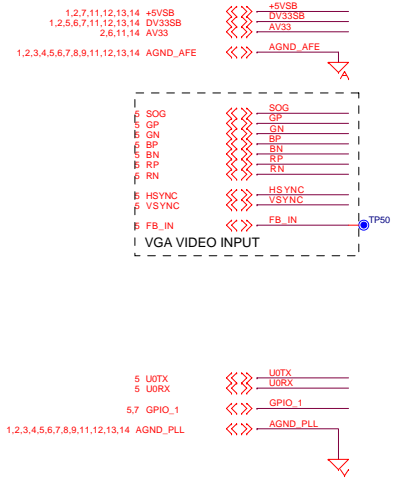
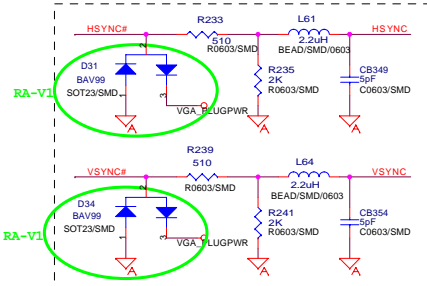
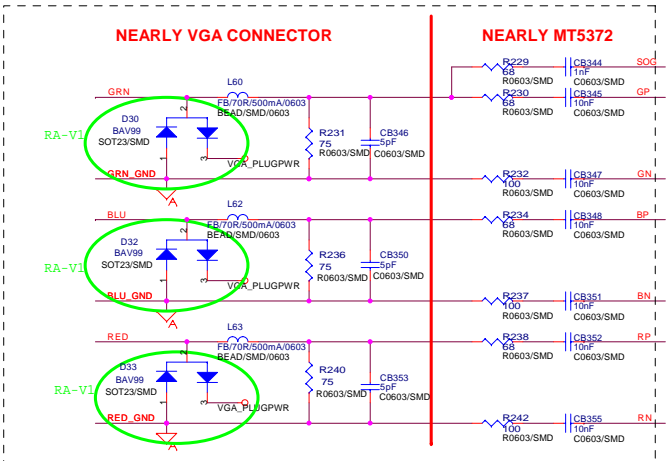
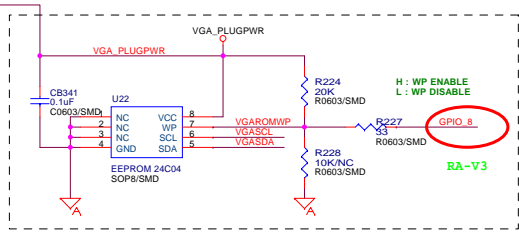
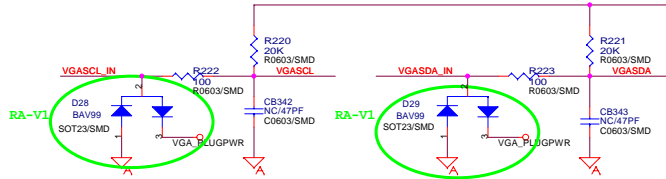
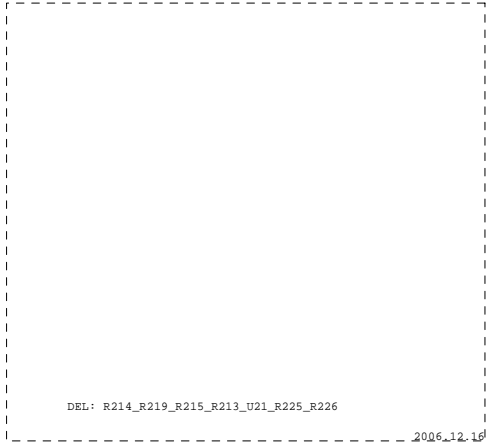
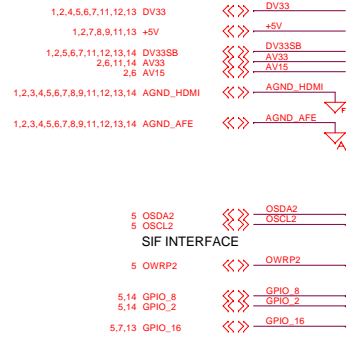
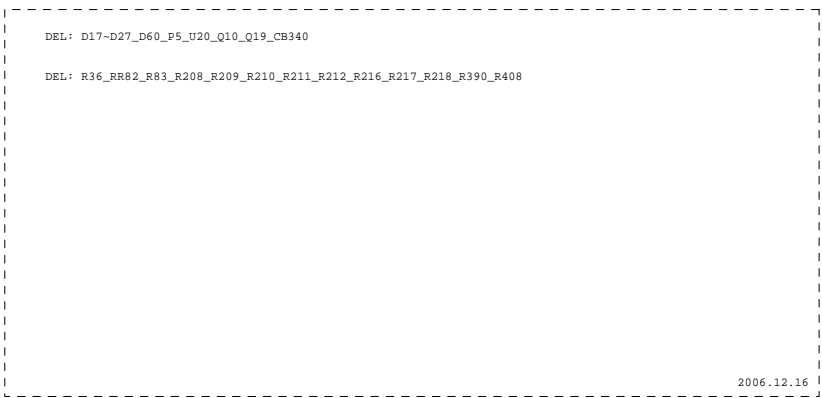
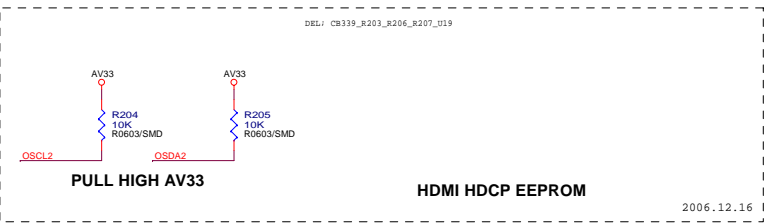
Checked: <Checker>

Date: Thursday, December 28, 2006 Sheet: 7 of 14





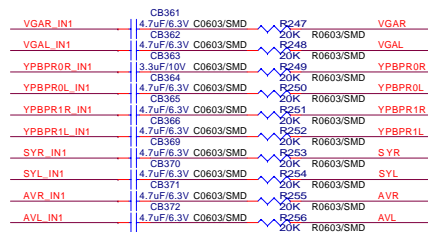




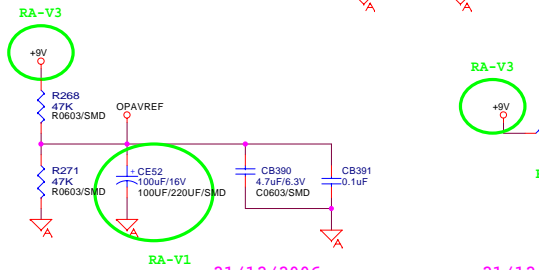
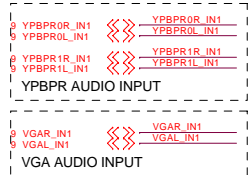
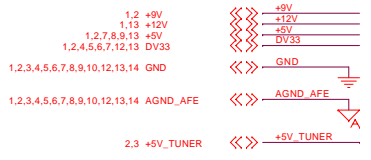
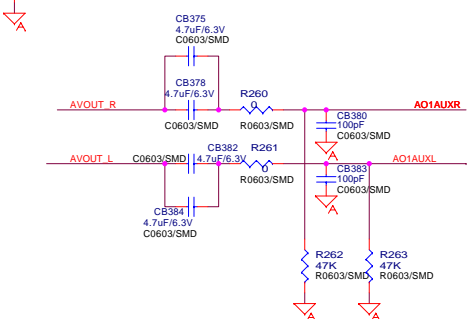
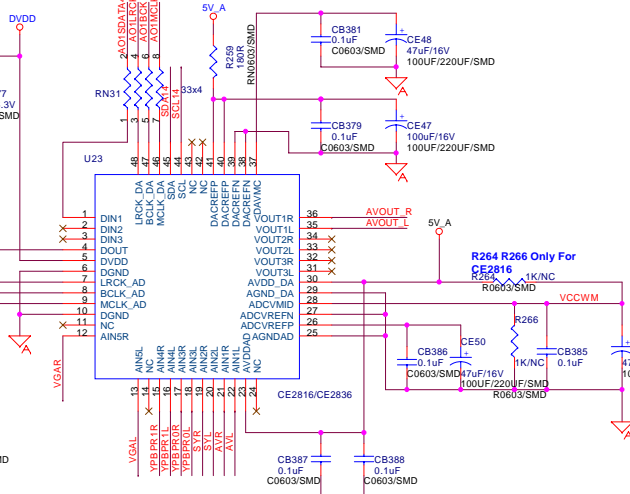
**ZhongShan KAWA Electronic Inc.**

Title: **HDMI I/VA INPUT**

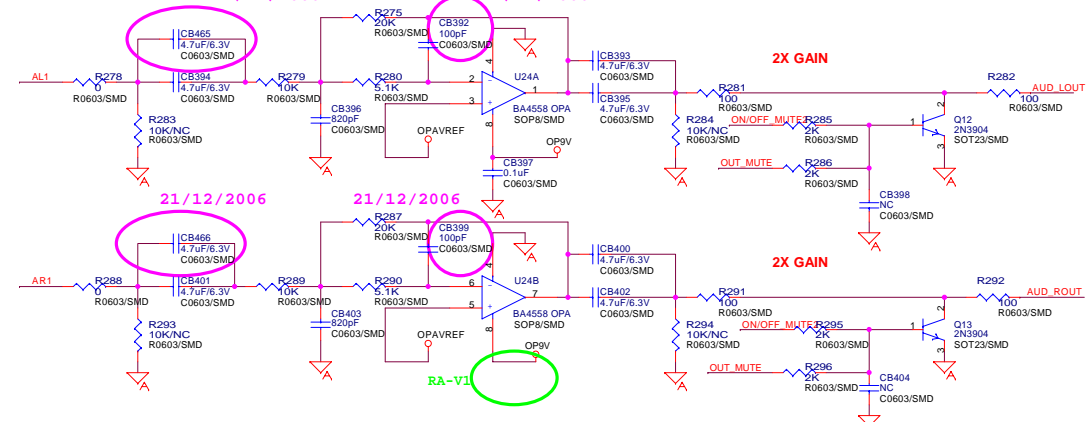
Size	Document Number	Drawn: <Designer>	Rev
Customer	<b>MT5371_V07</b>	Checked: <Checker>	1
Date:	Friday, December 29, 2006	Sheet	10 of 14



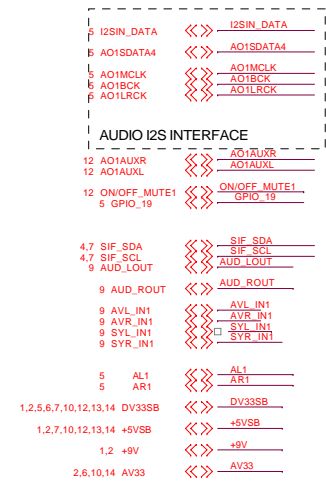
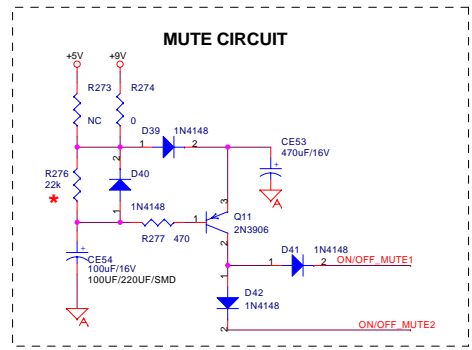
### AUDIO CODEC



### I2S UP TO 24-BIT DATA

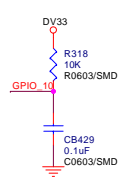
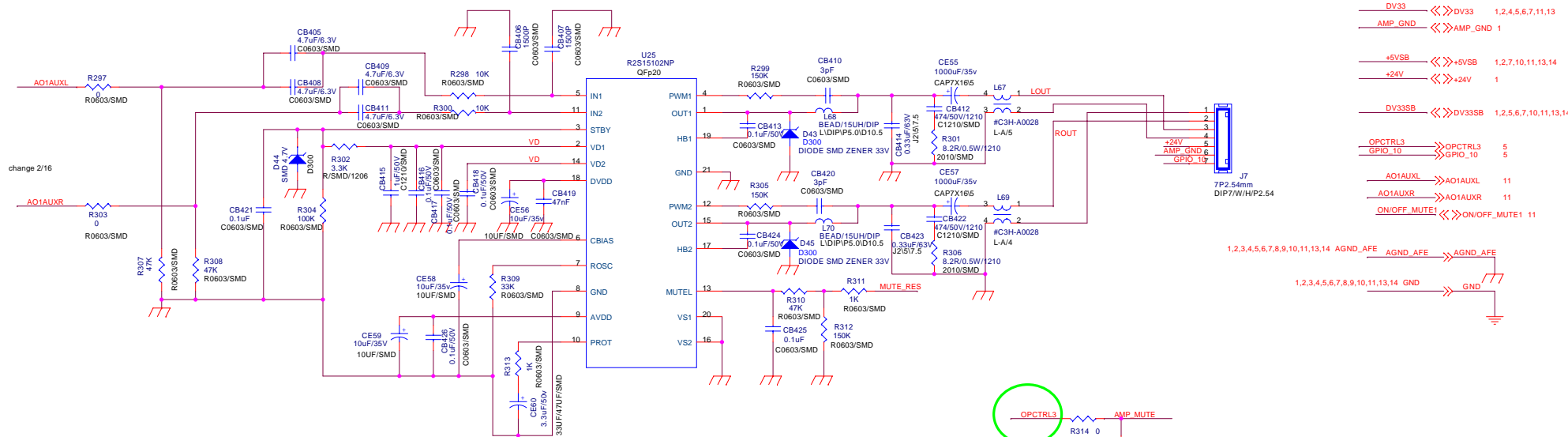


### INTERNAL AUDIO DAC OUTPUT

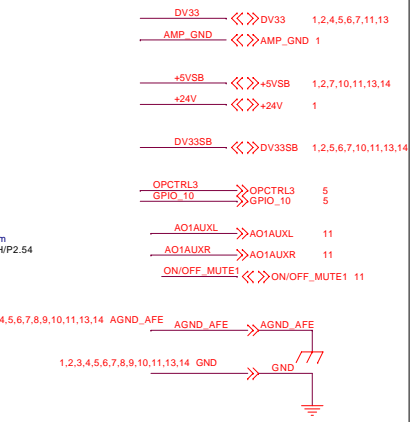
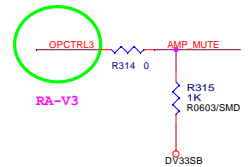
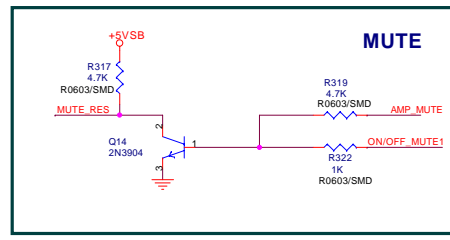
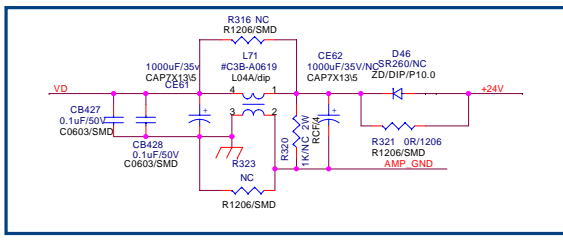


### ZhongShan KAWA Electronic Inc.

AUDIO CODEC			
Size	Document Number	Drawn: <Designer>	Rev
Customer	MT5371_V07	Checked: <Checker>	2
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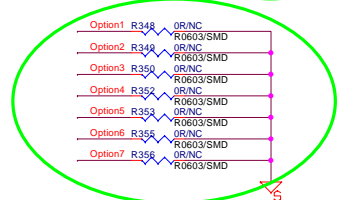
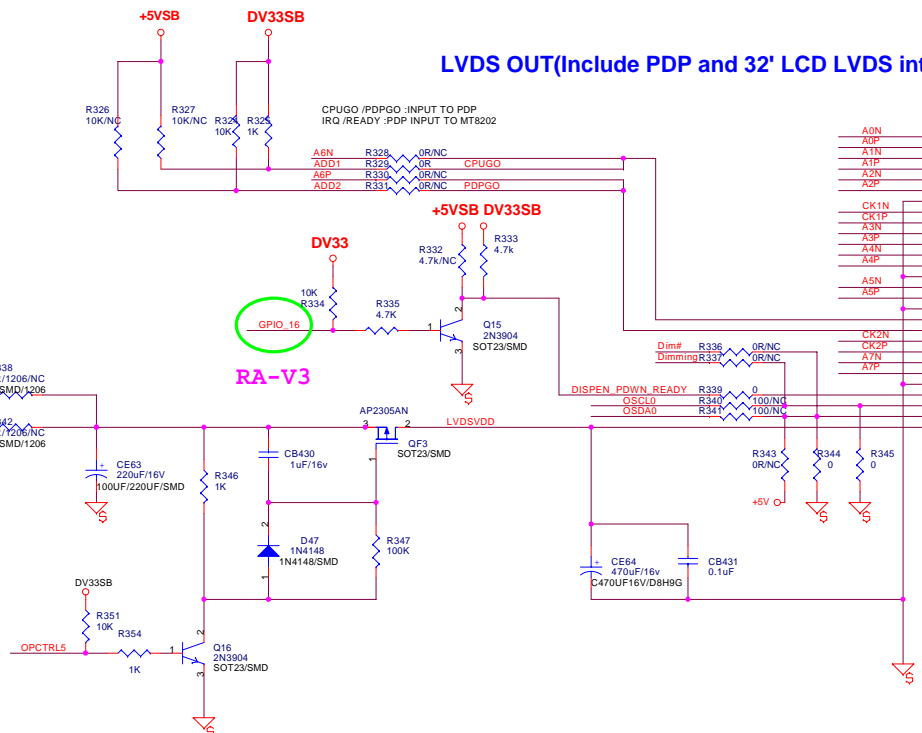
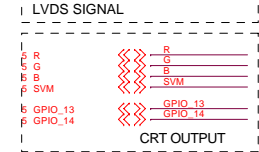
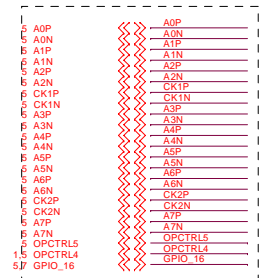
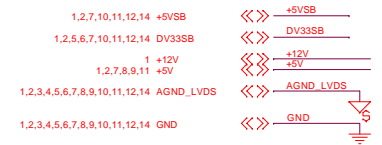
GPIO8: SPEAKER SWITCH(INTERNAL OR EXTERNAL)



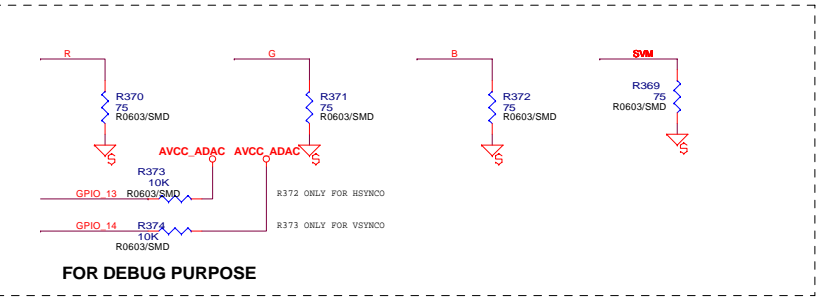
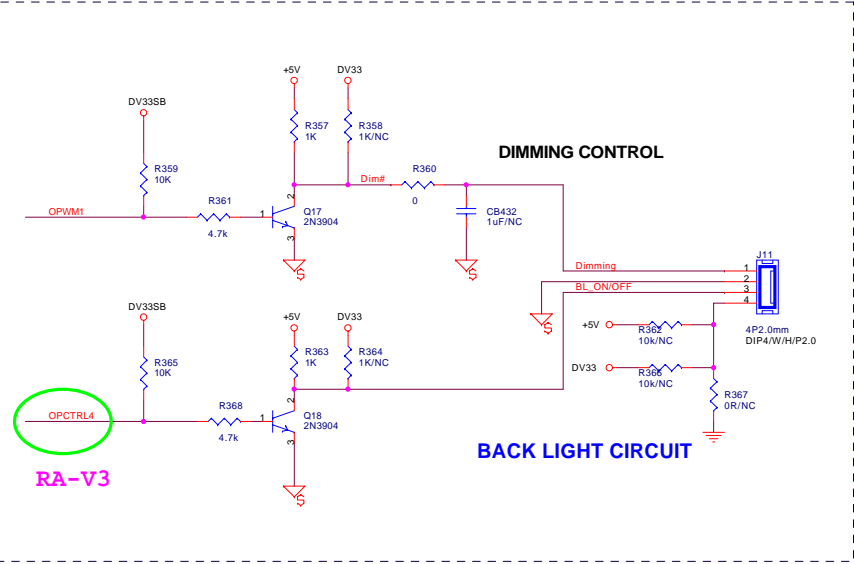
<b>ZhongShan KAWA Electronic Inc.</b>			
Title	<b>AUDIO AMP</b>		
Size	Document Number	Drawn: <Designer>	Rev
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Date:	Friday, December 29, 2006	Sheet	12 of 14

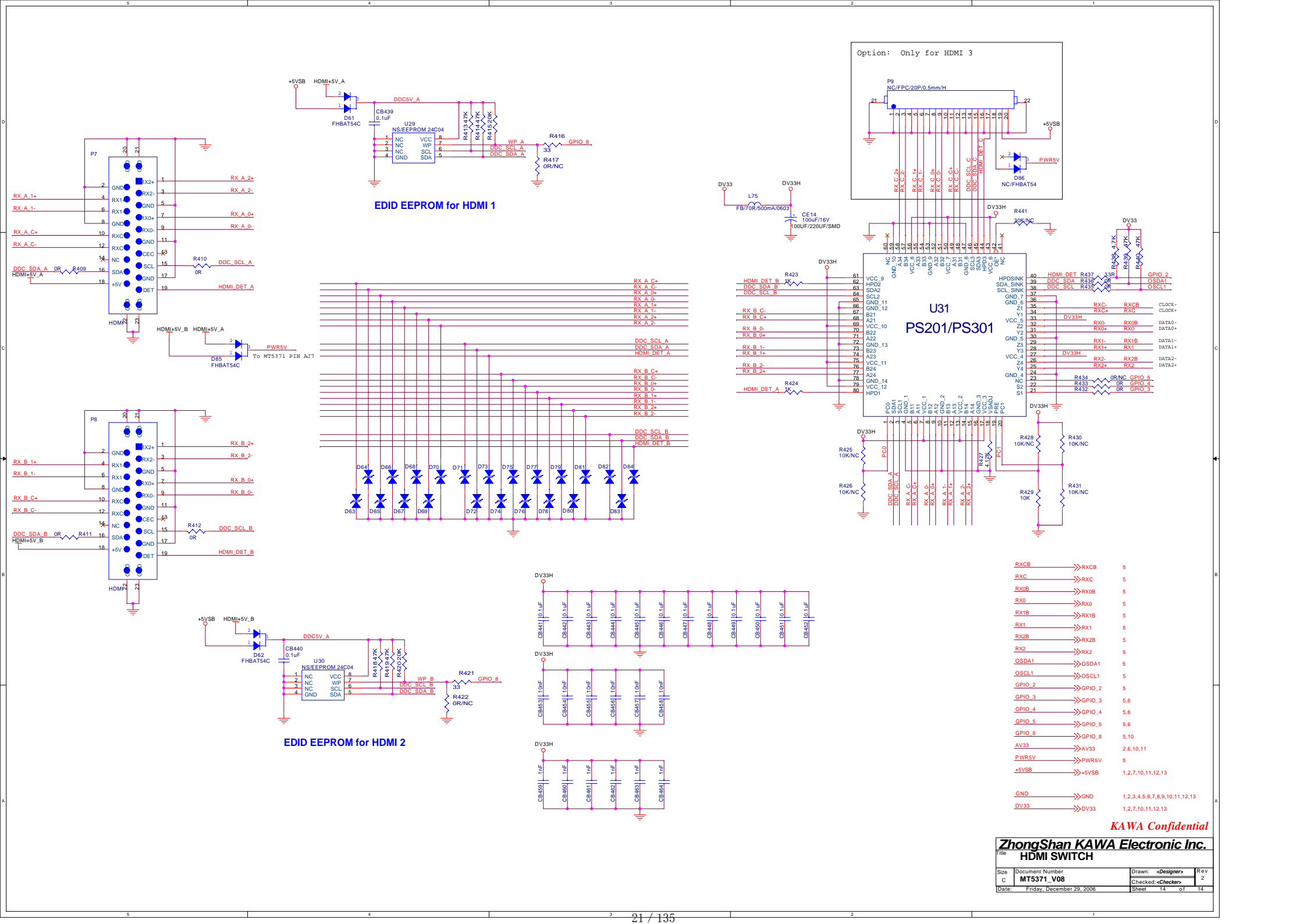
# LVDS OUT(Include PDP and 32' LCD LVDS interface)

## RA-V2



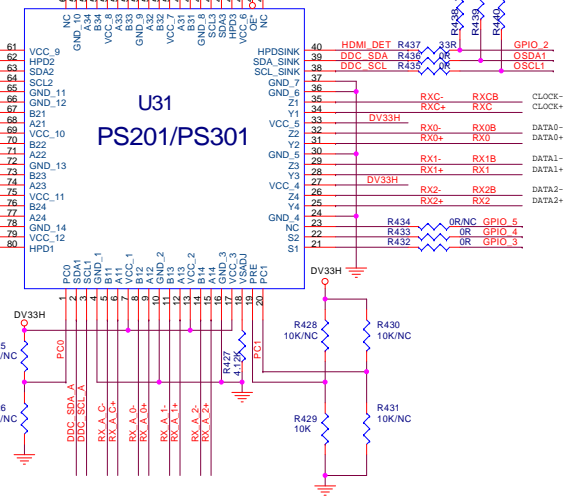
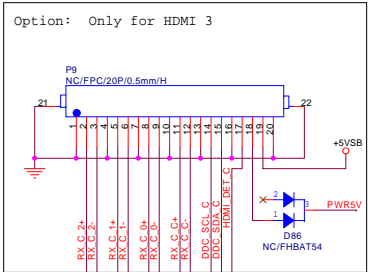
LO => LVDS POWER OFF  
 HI => LVDS POWER ON





EDID EEPROM for HDMI 1

EDID EEPROM for HDMI 2



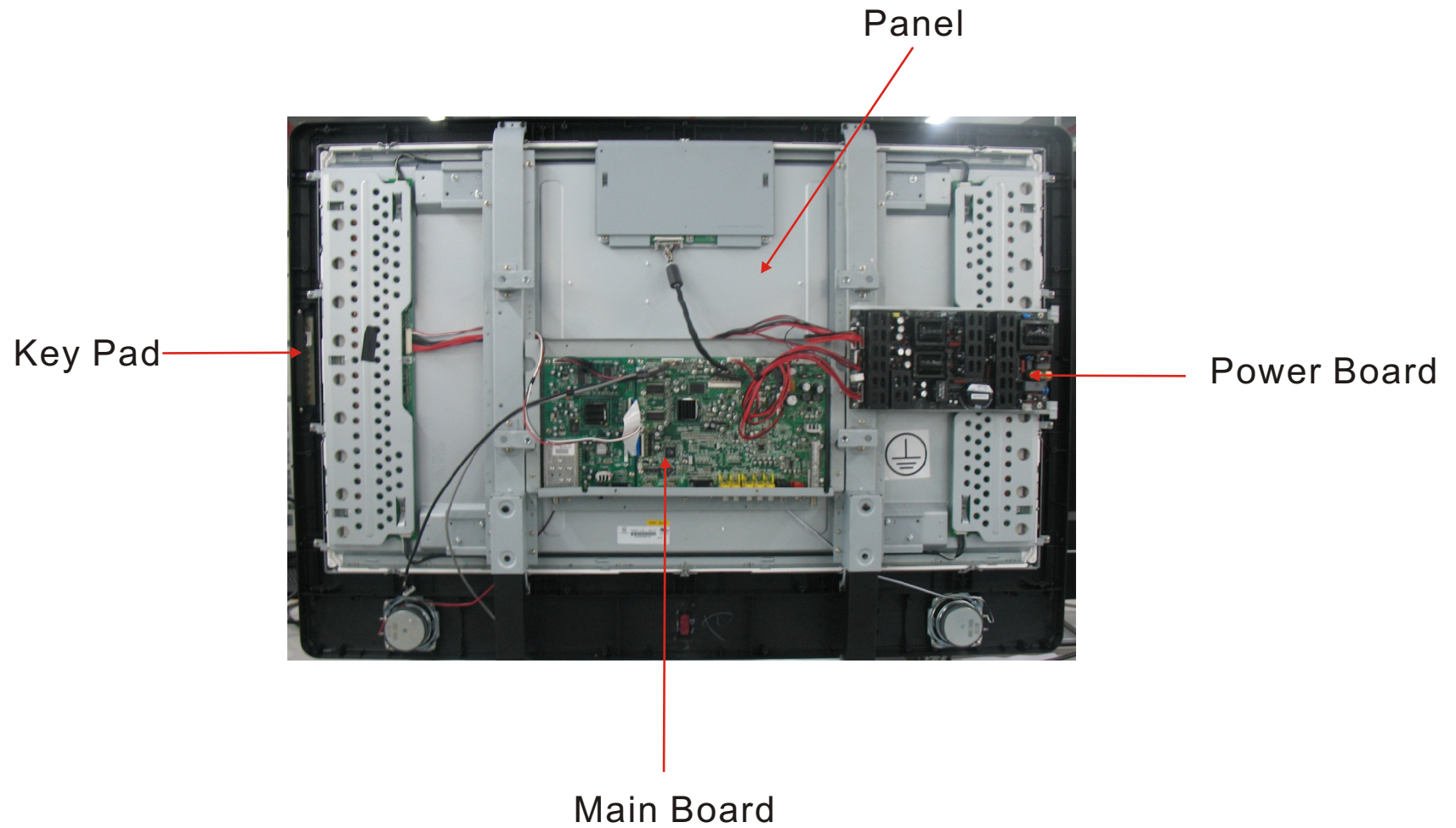
RXCB	>>>	RXCB	5
RXC	>>>	RXC	5
RX0B	>>>	RX0B	5
RX0	>>>	RX0	5
RX1B	>>>	RX1B	5
RX1	>>>	RX1	5
RX2B	>>>	RX2B	5
RX2	>>>	RX2	5
OSDA1	>>>	OSDA1	5
OSCL1	>>>	OSCL1	5
GPIO_2	>>>	GPIO_2	5
GPIO_3	>>>	GPIO_3	5.6
GPIO_4	>>>	GPIO_4	5.6
GPIO_5	>>>	GPIO_5	5.6
GPIO_8	>>>	GPIO_8	5.10
AV33	>>>	AV33	2.6,10,11
PWR5V	>>>	PWR5V	5
+5VSB	>>>	+5VSB	1,2,7,10,11,12,13
GND	>>>	GND	1,2,3,4,5,6,7,8,9,10,11,12,13
DV33H	>>>	DV33H	1,2,7,10,11,12,13

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HDMI SWITCH

Size	Document Number	Drawn: <Designer>	Rev
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# Parts position





## **Basic operation of TFT-LCD**

- 1. After turning on power switch, PSU board sends 5Vst-by Volt to Main IC MT5371 waiting for ON signals from Key Switch or Remote Receiver.**
- 2. When the ON signal from Key Switch or Remote Receiver is detected, MT5371 will send ON Control signals to Power. Then Sub PSU sends 5Vsc, 9Vsc, 24V to PCBs working.**
- 3. If some abnormal signals are detected (for example: over volts, over current, over temperature and under volts), the system will be shut down by Power off.**

## Main IC Specifications

- MT537x Application Note
- MT5112BD
- CE2836  
24-bit, 192KHz. CODEC: 6 ch DAC, 5 Input Mux Stereo ADC
- R2S15102NP  
Digital Power Amplifier R2S15102NP



MT537x Application Note

*Specifications are subject to change without notice*

**MT537x**

**Application Note**

V 0.5

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## 1. Revision History

Date	Description	Version
2006/05/18	Initial Version (Draft)	V.0.3
2006/05/27	Updated Power Load Power On/Off Timing	V.0.4
2006/06/06	Update On/Off Timing	V.0.5

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## 2. MT537x Feature

**MediaTek MT537x** is a highly integrated SOC which include DTV backend decoder and TV controller. MT537x support transport de-multiplexer, MPEG-2 video decoder, AC3 audio decoder, LVDS transmitter, TV decoder. The MT537x enables consumer electronics manufactures to build high quality, feature-rich DTV.

**World-Leading Video Technology:** MT537x embedded the MDDi deinterlacer to generate very smooth picture quality for motion. 3D comb filter also recover very high detail for still picture. The special color processing technology provided favorite and natural color for TV.

**Rich Features for High Value Product:** To enrich the features of DTV, MT537x support HDMI receiver, PIP/POP, memory card and DV decoding.

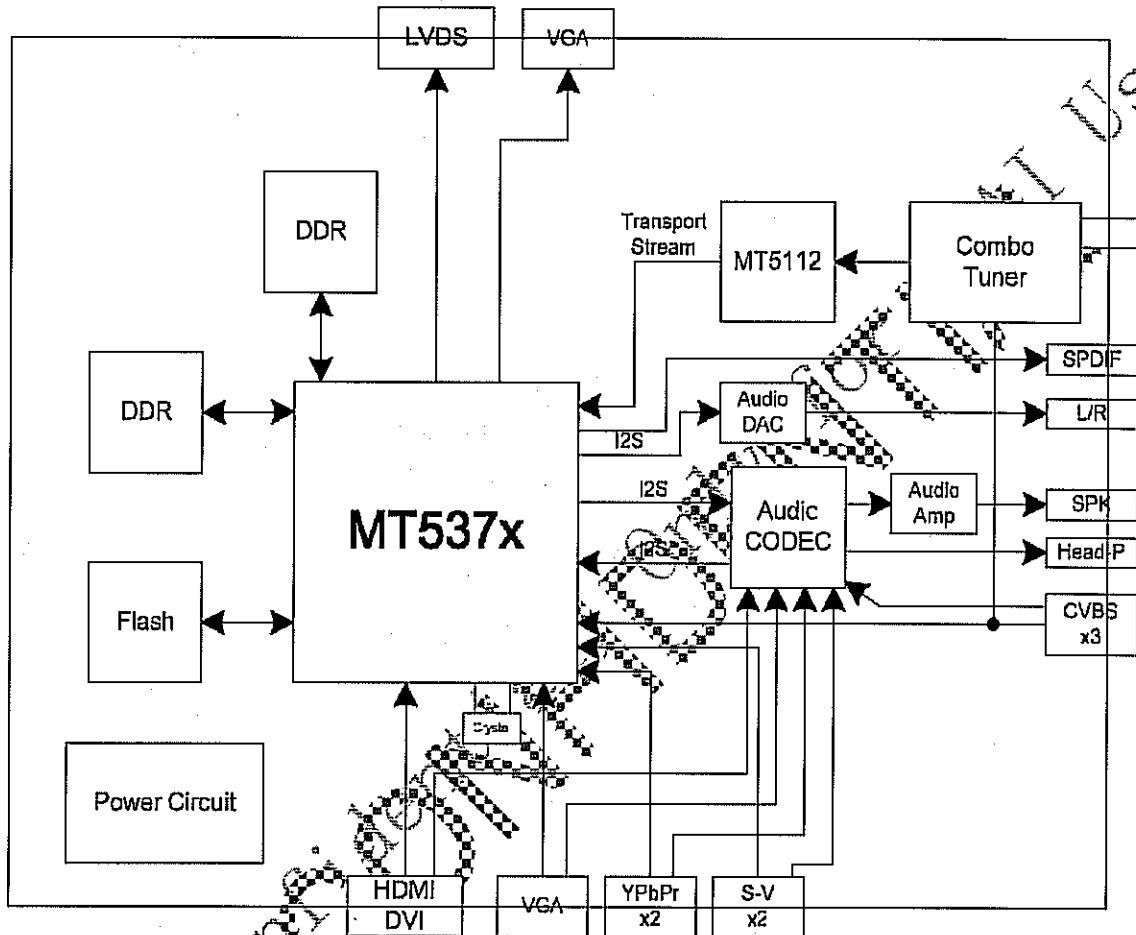
**Credible Analog Technology:** The MT537x integrated with high speed VGA ADC, high resolution Video/Audio ADC, 90db Audio DAC and 12-bit Video DAC. It will provide very fine quality for TV.

## 3. DTV System Block (Reference Design)



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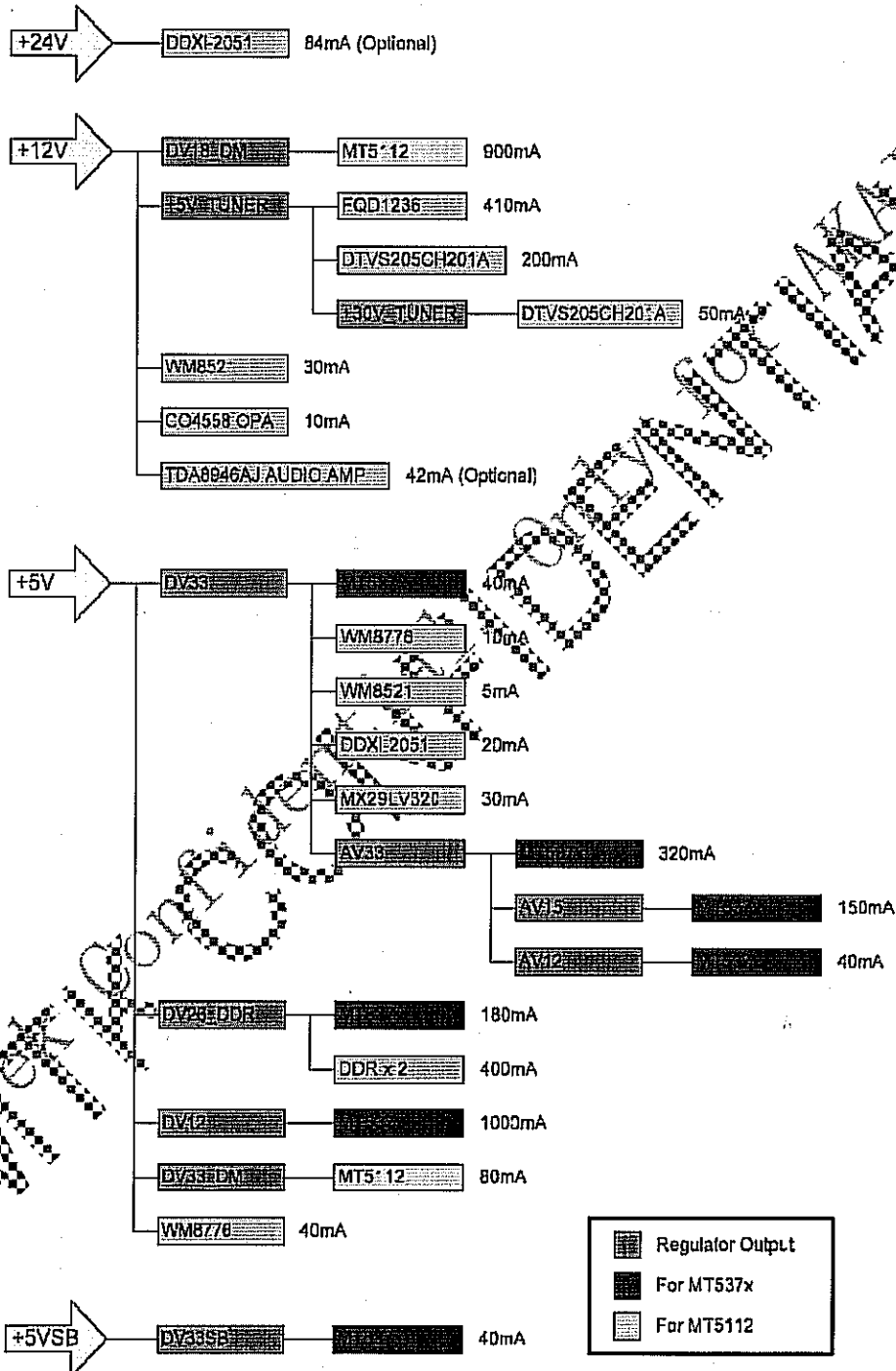
#### 4. DTV System Power Load (Based on Reference Design)



# MT537x Application Note

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## 5. MT537x Power Consumption

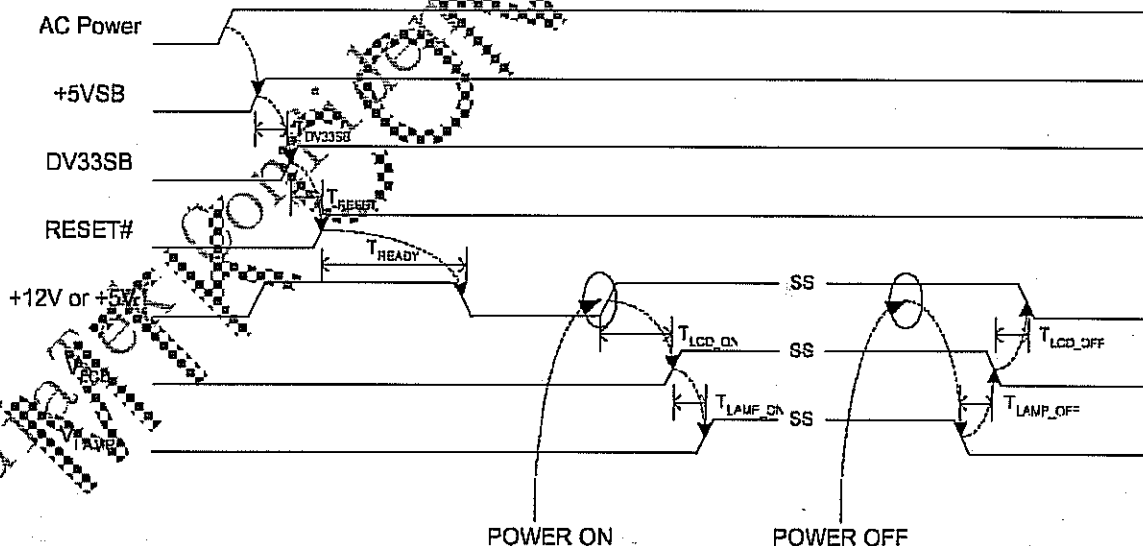
Under Measurement

Power	Current (mA)	Power Consumption (mW)	RS
DV33	40	132	
AV33	320	1056	
DV26	180	468	
AV15	150	225	
DV12	1000	1200	
AV12	40	48	
DV33SB	40	132	

Note :

Due to We are Under Integration, the Power Consumption Just for Reference. The Power may Increase after Full Function Play

## 6. MT537x Power On / Off Timing



Description	Symbol	Min	TPY	Max	Units	PS
DV33SB Power Ready	$T_{DV33SB}$	0			ms	





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Power-on Reset Period	T <sub>RESET</sub>	10		ms	
MT537x Boot Ready	T <sub>READY</sub>		20	ms	
LCD Power On	T <sub>LCD ON</sub>			ms	Depend-on Panel
LCD Lamp On	T <sub>LAMP ON</sub>			ms	Depend-on Panel
LCD Lamp Off	T <sub>LAMP OFF</sub>			ms	Depend-on Panel
LCD Power Off	T <sub>LCD OFF</sub>			ms	Depend-on Panel

## 7. MT537x Diagnostic Program CLI Commands

Under Development

- cd – change current directory  
ex. cd.av – change the directory to AV directory
- do – repeat command  
do "number of times"  
ex. do
- read (r) – memory read  
r "address" "number of bytes"  
ex. r 0x2000d068 8 ← read 8 bytes data from 0x2000d068 address
- write (w) – memory write  
w "address" "data"  
ex. w 0x2000d068 0x12345678 ← write 0x12345678 data to 0x2000d068 address
- basic (b) – basic command
  - stop - stop RS232 transparent mode (set to normal mode)  
ex. b.stop ← set RS232 to normal mode
  - sv – system mode detection  
ex. b.sv ← to detect the system mode
  - reboot – system reboot / restart  
ex. b.reboot ← reboot the system

## 8. MT537X Debug Flow

Under Development

## 9. MT537x NOR Flash Supported



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Brand	IC Order Number	Size	Description
MXIC	MX29LV320ABTC-70	32Mbits	Under Testing
MXIC	MX29LV320ABTC-90	32Mbits	Under Testing
MXIC	MX29LV320ATTC-70	32Mbits	Under Testing
MXIC	MX29LV320ATTC-90	32Mbits	Under Testing
MXIC	MX29LV320BBTC-70	32Mbits	Under Testing
MXIC	MX29LV320BBTC-90	32Mbits	Under Testing
MXIC	MX29LV320BTTC-70	32Mbits	Under Testing
MXIC	MX29LV320BTTC-90	32Mbits	Under Testing
MXIC	MX29LV320BTC-70	32Mbits	Under Testing
MXIC	MX29LV320BTC-90	32Mbits	Under Testing
MXIC	MX29LV320TTC-70	32Mbits	Under Testing
MXIC	MX29LV320TTC-90	32Mbits	Under Testing
Winbond	W19B320ABT7H	32Mbits	Under Testing
ST	M29W320DT-90	32Mbits	Under Testing
ST	M29W320DT-70	32Mbits	Under Testing
ST	M29W320DB-70	32Mbits	Under Testing
Spansion	S29GL032-90T	32Mbits	Under Testing

### 10. MT537x DDR/2 Supported

Brand	IC Order Number	DDR Type	Description
Nanya	NT5DS32M16BT-5T	DDR	32Mx16, Under Testing
ProMOS	V58C2512164SB5	DDR	32Mx16, Under Testing
Infineon	HYB25DC512160CE-5	DDR	32Mx16, Under Testing
Hynix	HY5DU121622ALT-D43	DDR	32Mx16, Under Testing
MIRA	P2S12D40CTP-G5	DDR	32Mx16, Under Testing
Micron	MT46V32M16TG-5B	DDR	32Mx16, Under Testing
PSC	A2S56D40CTP-G5	DDR	16Mx16, Under Testing
Nanya	NT5DS16M16CS-5T	DDR	16Mx16, Under Testing
ProMOS	V58C2256164SCI5	DDR	16Mx16, Under Testing
Hynix	HY5DU561622CT-5	DDR	16Mx16, Under Testing



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ELPIDA	DD2516AKTA-6B-E	DDR	16Mx16, Under Testing
Infineon	HYB25DC256160CE-5	DDR	16Mx16, Under Testing
MIRA	P2S56D40CTP-G5	DDR	16Mx16, Under Testing
Micron	MT46V16M16TG-5B	DDR	16Mx16, Under Testing
Samsung	K4D551638F-LC50	GDDR	16Mx16, Under Testing
PSC	A3R12E4FDF-G6EA	DDR2	32Mx16, Under Testing
Infionin	HYB18TC512160AF-3S	DDR2	32Mx16, Under Testing
ProMOS	V59C1512164QA-3	DDR2	32Mx16, Under Testing
Nanya	NT5TU32M16AG-3C	DDR2	32Mx16, Under Testing
Hynix	HY5PS121621LF-Y5	DDR2	32Mx16, Under Testing
Micron	MT47H32M16-3	DDR2	32Mx16, Under Testing
Infionin	HYB18TC256160AF-3S	DDR2	16Mx16, Under Testing
Hynix	HY5PS561621LF-Y5	DDR2	16Mx16, Under Testing
Micron	MT47H16M16-3	DDR2	16Mx16, Under Testing

### 11. MT537x PCB Layout Guidelines

- 4-layer PCB Design (TOP / GND / POWER / BOTTOM)
- Power Arrangement
  1. DV33 : Supply to MT537x Digital and Peripheral
  2. AV33 : Supply to MT537x Analog
  3. DV25/DV18 : Supply to MT537x and DDR/2
  4. AV15 : Supply to MT537x Video Front-end 1 (YPbPr/RGB)
  5. AV15\_DAC : Supply to MT537x Video DAC
  6. DV12 : Supply to MT537x Digital
  7. AV12 : Supply to MT537x Analog
- Power Plane
  1. The Power has High Priority in Layer 3
  2. If There are No Enough Plane in Layer 3, the Power Line Should be Routed Wider (Component Side Has High Priority)
  3. Be Care the Power Return Path, Especially for Large Power
  4. The Switching Power Should leave alone the Analog Portion
- Ground Plane
  1. In General, We Use Only One Ground (Don't Divided) in Layer 2
  2. You May Have Independent Ground if There are Large Power Consumption in Your Design, for Example - Digital Audio AMP. But You Should Note That the

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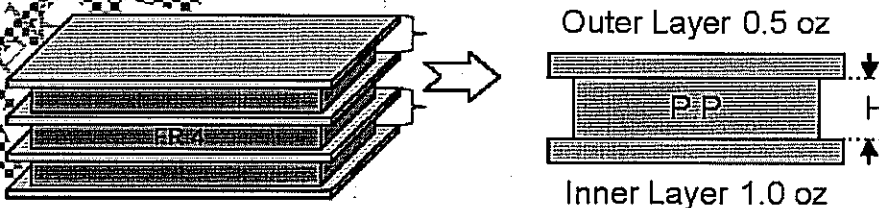
Signal Return Path

3. Please Flush the Copper both in Component and Solder Sides
- The Bypass Cap. Should be Located as Close to IC's Power Pin as Possible
  - The VCXO or Crystal Should be Located as Close to IC as Possible
  - The Video Termination Resistor Should be Closed to Connector
  - The Video AC-couple Cap. Should be Closed to MT537x
  - Video Signal YPbPr and RGB Don't Cross with Other Signal (Must)
  - Video Signal CVBS and S-Video Don't Cross with Other Signal as Possible. If Need, Please Add Ground Shielding (Guard Trace) on the Side of the Video
  - Audio Signal (Analog) Don't Cross with Other Signal as Possible. If Need, Please Add Ground Shielding (Guard Trace) on the Side of the Audio
  - To Avoid Routing any Traces on the Ground or Power Plane
  - Digital Signal Width Please Use 6 mil
  - DDR/2 Layout – Please Follow the Layout Guide Described Below or Copy from MTK's Library to Speed-up the Design Time
  - If You had Re-layout the DDR/2, Please Provide the Layout File for DDR/2 SI Simulation (Familiar with PowerPCB Format)
  - HDMI / LVDS Layout – Please Follow the Layout Guide Described Below

## 12. MT537x DDR/2 Layout Guide

### 12.1 4 Layer PCB Layout Constraints

#### 12.1.1 Board Stack-up



PCB Stackup – 4 Layers



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The outer layers of the PCB were designated to the mainly signal routings by default, and normally were chosen to have the 0.5 oz Cu foil with plated 0.5 oz copper, and the inner layers was designated to be 1.0 oz at the PCB manufacturing step.

The dielectrics between conductors were as the isolators, which were used to separate the conductors. By the micro-strip line architecture of system memory signals, the target impedance was desired to have 55Ω +/- 10%. Please refer to the table below for your PCB design and recommendation. The default design was 6 mil trace width with 4.5 mil height dielectrics.

4 Layer PCB Stack-up Configurations

PCB Parameter			
Trace Width (mil)	H (mil)	Target Impedance (Ω)	Tolerance
5	4.5	56	10%

Please request the PCB manufactory to follow the FR4 stack-up as below

Description	Material	Height (mil)	PS
Conductor		0.5 oz	
Medium	<input type="checkbox"/> No Assigned <input checked="" type="checkbox"/> Assigned	4.5	2116
Conductor		1 oz	
Medium		47.6	
Conductor		1 oz	
Medium		4.5	
Conductor		0.5 oz	

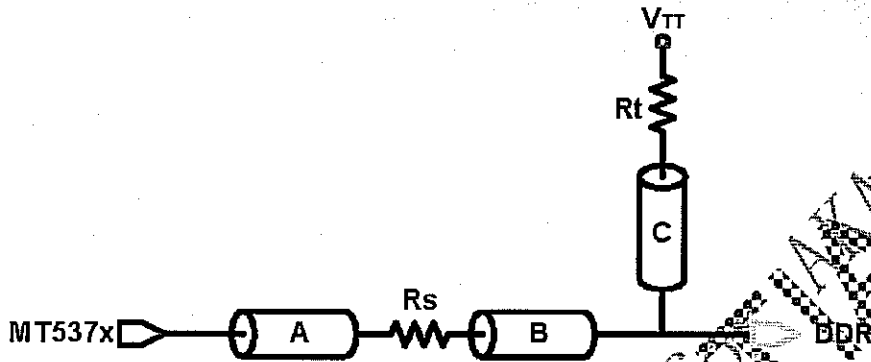
12.2 System DDR-Memory Solution Space

Refer to the diagrams below to the topologies of the DDR signals, and the actual dimension specifications were listed of the tables

12.2.1 DDR Signal Topology – 1 (DS / DQS / DQM)

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DDR Signal Topology - 1

Signal		DQ	DQS	DQM
Trace (mil)	Width (W)	5	5	5
	Spacing	8 or Above	8 or Above	8 or Above
Trace Length (inch)	A	Min.	0.2	0.2
		Max.	1	1
	B	Min.	0.2	0.2
		Max.	1.2	1.2
	C	Min.	0.1	0.1
		Max.	0.5	0.5
A+B	Min.	0.4	0.4	
	Max.	2	2	
$R_s (\Omega)$		47	47	47
$R_t (\Omega)$		75	75	75

Note :

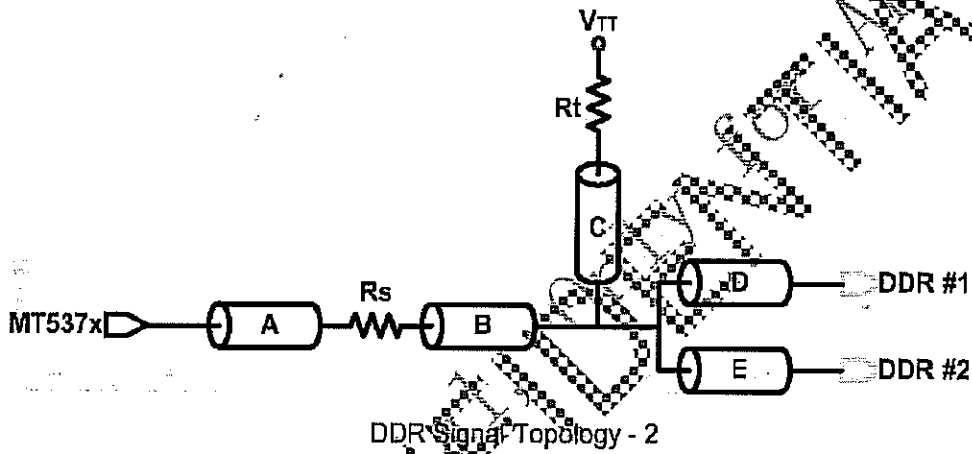
1. Keep the difference of the trace length of the same data signal groups within about 200 mils as possible.
2. Keep the difference of the data signal groups within 200 mils as possible (The longest signal trace to the shortest signal trace).
3. Placing the damping resistor close to the MT537x.
4. Placing the termination resistor close to the memory as possible.
5. Put an integrated plane as the return path to the signals beneath the data signals.
6. When the signal need to change layers, and the reference paths beneath

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the signal are not continued, placing the bypass capacitors nearing to the vias where are the points to change layers and connecting the capacitors to the different reference paths.

12.2.2 DDR Signal Topology – 2 (Address and Command)



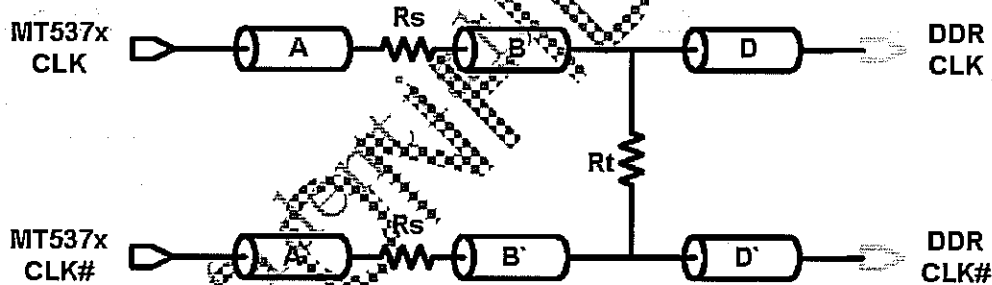
Signal		RA / BA	CS# / CAS# / RAS# / WE#	CKE
Trace (mil)	Width (W)	5	5	5
	Spacing	8 or Above	8 or Above	8 or Above
Trace Length (Inch)	A	Min.	0.2	0.2
		Max.	1.2	1.2
	B	Min.	0.2	0.2
		Max.	2	2
	C	Min.	0	0
		Max.	0.5	0.5
	D / E	Min.	0.2	0.2
		Max.	1.2	1.2
A+B+D (or E)	Min.	0.6	0.6	
	Max.	4.2	4.2	
Rs (Ω)		22	22	22
Rt (Ω)		75	75	75

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Note :

1. Keep the difference of the branches' length (D / E) of the dual loads signal within 100 mils.
2. Placing the damping resistor close to the MT537x.
3. Put the termination resistor close to the crossing point of the branches.
4. Reserving more spacing to the periodic signal ( as clock ) if signal was critical and there weren't the guard traces.
5. Put an integrated plane as the return path to the signals beneath the address / command signals.
6. When the signal need to change layers, and the reference paths beneath the signal are not continued, placing the bypass capacitors hearing to the vias where are the points to change layers and connecting the capacitors to the different reference paths.

12.2.3 DDR Signal Topology – 3 (Clock Pair)



DDR Signal Topology - 3

Signal		CLK / CLK#	
Trace (mil)	Width	5	
	Spacing	8 or Above	
Trace Length (inch)	A	Min.	0.2
		Max.	1
	B	Min.	0.2
		Max.	1
	D	Min.	0.2
		Max.	1.2
A+B+D	Min.	0.6	





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	Max.	2.6
Rs ( $\Omega$ )		47
Rt ( $\Omega$ )		100

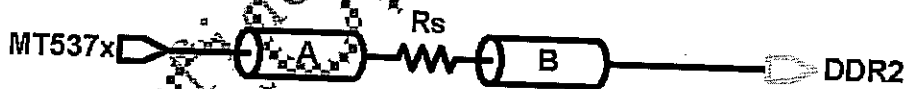
Note :

1. The trace length of A / A', B / B' , D / D' should be as equal as possible.
2. Keep the trace difference between CLK / CLK# in +/- 100 mils.
3. Keep the trace difference between DQ / DQS / DQM and CLK in +/- 200 mils.
4. Keep the trace difference between RA / BA / CS# / CAS# / RAS# / WE# / CKE and CLK in +/- 1000 mils.

### 12.3 System DDR2 Memory Solution Space

Refer to the diagrams below to the topologies of the DDR2 signals, and the actual dimension specifications were listed of the tables.

#### 12.3.1 DDR2 Signal Topology - 1 (DQ and DQM)



DDR2 Signal Topology - 1

Signal		DQ	DQM
Trace (mil)	Width (W)	5	5
	Spacing	8 or Above	8 or Above
Lengt	A	0.2	0.2
	Max.	1	1
B	Min.	0.2	0.2



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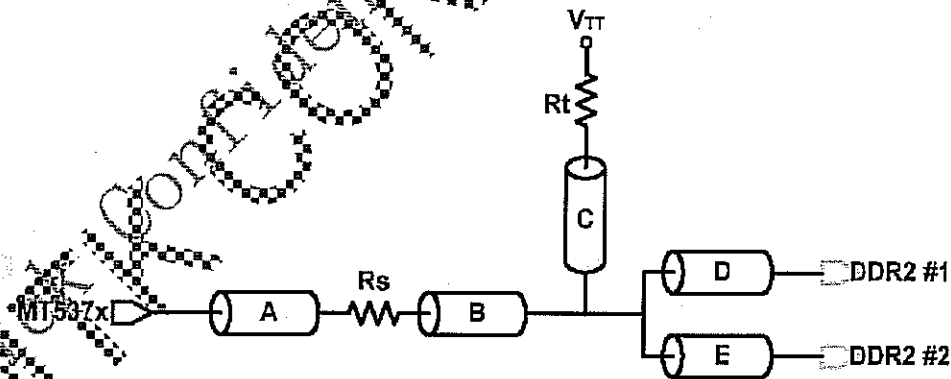
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A+B	Max.	1.2	1.2
	Min.	0.4	0.4
	Max.	2	2
Rs (Ω)		22	22

Note :

1. Keep the difference of the trace length of the same data signal groups within about 200 mils as possible.
2. Keep the difference of the data signal groups within 200 mils as possible (The longest signal trace to the shortest signal trace).
3. Placing the damping resistor close to the MT537x.
4. Placing the termination resistor close to the memory as possible.
5. Put an integrated plane as the return path to the signals beneath the data signals.
6. When the signal need to change layers, and the reference paths beneath the signal are not continued, placing the bypass capacitors nearing to the vias where are the points to change layers and connecting the capacitors to the different reference paths.

12.3.2 DDR2 Signal Topology – 2 (Address and Command)



DDR2 Signal Topology - 2

Signal	RA / BA	CS# / CAS# / RAS# / WE#	CKE
Trace (mil)	Width (W)	5	5



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		Spacing	8 or Above	8 or Above	8 or Above
Trace Length (inch)	A	Min.	0.2	0.2	0.2
		Max.	1.2	1.2	1.2
	B	Min.	0.2	0.2	0.2
		Max.	2	2	2
	C	Min.	0	0	0
		Max.	0.5	0.5	0.5
	D / E	Min.	0.2	0.2	0.2
		Max.	1.2	1.2	1.2
	A+B+D (or E)	Min.	0.6	0.6	0.6
		Max.	4.2	4.2	4.2
Rs ( $\Omega$ )			22	22	22
Rt ( $\Omega$ )			75	75	75

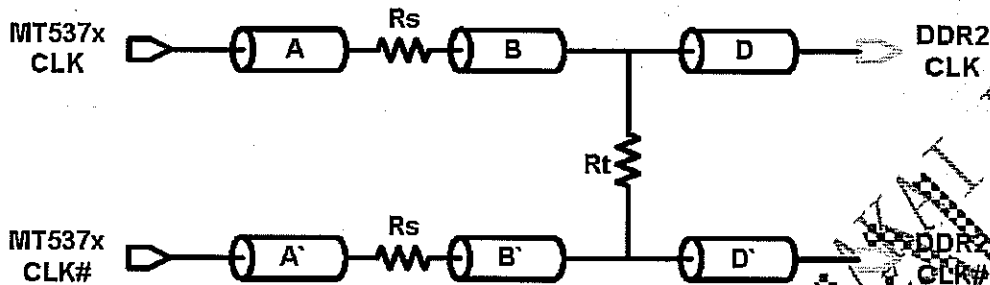
Note :

1. Keep the difference of the branches length ( D / E ) of the dual loads signal within 100 mils.
2. Placing the damping resistor close to the MT537x.
3. Put the termination resistor close to the crossing point of the branches.
4. Reserving more spacing to the periodic signal ( as clock ) if signal was critical and there weren't the guard traces.
5. Put an integrated plane as the return path to the signals beneath the address / command signals.
6. When the signal need to change layers, and the reference paths beneath the signal are not continued, placing the bypass capacitors nearing to the vias where are the points to change layers and connecting the capacitors to the different reference paths.

### 12.3.3 DDR2 Signal Topology – 3 (Clock and DQS)

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DDR2 Signal Topology - 3

Signal		CLK / CLK#	DQS / DQS#
Trace (mil)	Width (W)	5	5
	Spacing	8 or Above	8 or Above
Trace Length (inch)	A	Min.	0.2
		Max.	1
	B	Min.	0.2
		Max.	1
	D	Min.	0.1
		Max.	1.2
A+B+D	Min.	0.6	
	Max.	2.6	
Rs(Ω)		22	22
Rt(Ω)		100	NS

Note :

1. The trace length of A / A', B / B', D / D' should be as equal as possible.
2. Keep the trace difference between CLK / CLK# in +/- 100 mils.
3. Keep the trace difference between DQ / DQS / DQM and CLK in +/- 200 mils.
4. Keep the trace difference between RA / BA / CS# / CAS# / RAS# / WE# / CKE and CLK in +/- 1000 mils.

## 13. MT537x HDMI / LVDS Layout Guide

### 13.1 HDMI / LVDS Signal PCB Layout Guideline

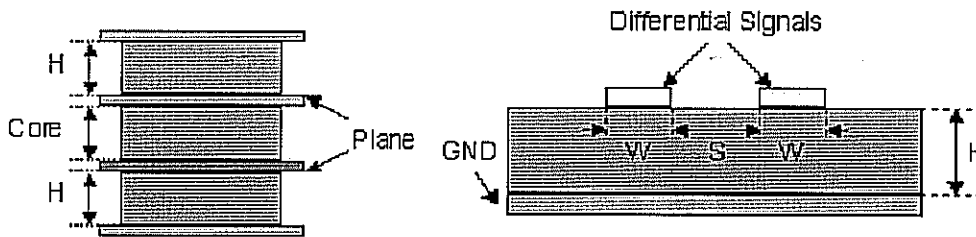
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For the other applications of the high-speed signal PCB design, below illustrated the topologies and constraints of the HDMI / LVDS or other differential signals that were achieved to the electrical requirements. Also refer to the form to the detail recommendations.

### 13.2 Multi-Layer PCB Design

By the default multi-layers PCB architecture, the inner layers were assigned to be the reference plane to the signals. For the signal integrity issues, the integrate plane would held to hold a good signal qualities when signal were proceeding on the signal traces. Refer to the below shown the stack up and the topology of the differential signals of the 4-layer PCB where the signals were routed of the outer layers.

#### 13.2.1 Signals without Guard Traces



HDMI / LVDS Signal Topology - 4 Layer

Variable	Nominal (mil)	Tolerance	Min. (mil)	Max. (mil)
Trace High (H)	4.5 (2116)			
Trace Width (W)	5	+ / - 1 mil	4	6
Spacing (S)	8 (mil)	+ / - 1 mil	9	7
Single Ended Trace Impedance	56Ω		61.6Ω	52.6Ω
Differential Trace Impedance	98Ω		109Ω	89.9Ω
Reference Plane	Ground	Ground	Ground	Ground

#### 13.2.2 Signals with Guard Traces

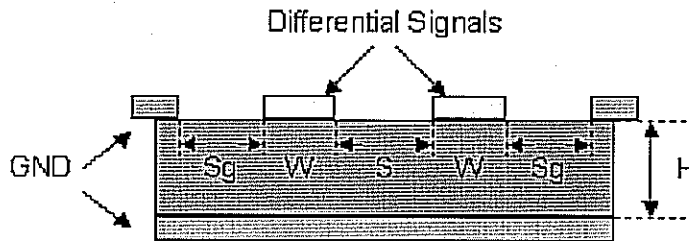
The other application was used the coplanar ground copper and surrounded the



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signals to achieve the noise shielding purpose. The figure shows the signal topology.

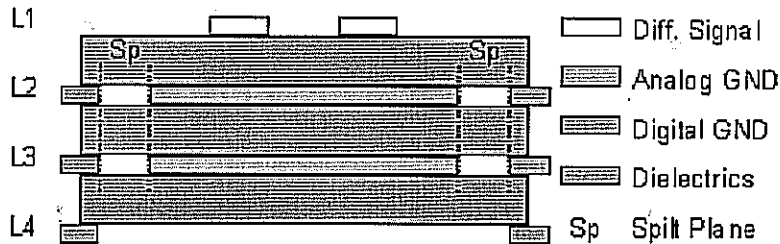


Differential Signal with Guard Trace

Variable	Nominal (mil)	Tolerance	Min. (mil)	Max. (mil)
Trace High (H)	4.5 (2116)			
Trace Width (W)	5	+ / - 1 mil	4	6
Spacing (S)	8 (mil)	+ / - 1 mil	9	7
Spacing to GND(Sg)	8 (mil)	+ / - 1 mil	9	7
Single Ended Trace Impedance	55Ω		60Ω	50.5Ω
Differential Trace Impedance	97Ω		107Ω	87Ω
Reference Plane	Ground	Ground	Ground	Ground

Note:

1. Keeping the spacing to the other signals as far as possible.
2. Keeping the spacing to different ground planes (Sp) more than 30 mils as possible as the below.



Cross-Section of Plane Designated



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## 14. MT537x BGA Soldering Information

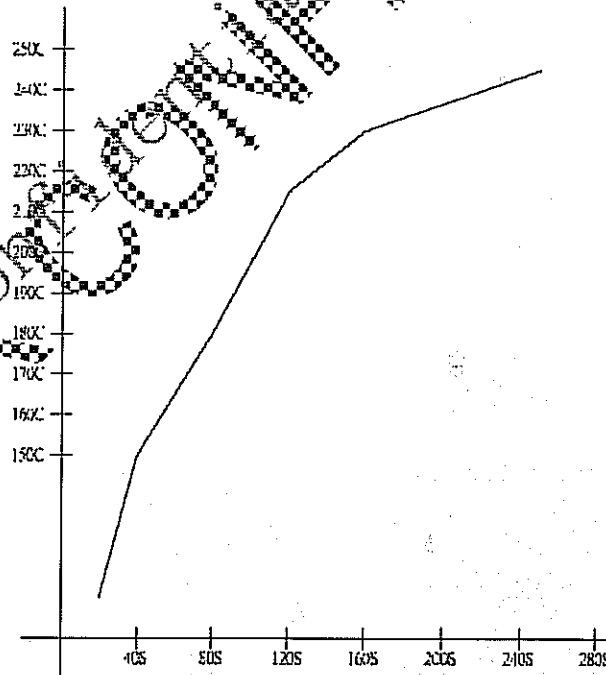
### 14.1 MT537xAG is Lead-Free Process

Element :

1. Sn : 95.5 %
2. Ag : 4 %
3. Cu : 0.3 %
4. Fusion Point : 228 °C.

### 14.2 Soldering Control (for Reference Only)

1. 150 °C : 40 Sec
2. 180 °C : 40 Sec
3. 215 °C : 40 Sec
4. 230 °C : 40 Sec
5. 245 °C : 90 Sec
6. 245 °C : 30 Sec





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### 15. US Terrestrial TV Channel Frequencies

Channel	TV Video Freq (MHz)	ATSC Center Freq (MHz)	Channel	Video Freq (MHz)	ATSC Center Freq (MHz)
2	55.25	57	36	603.25	605
3	61.25	63	37	609.25	611
4	67.25	69	38	615.25	617
5	77.25	79	39	621.25	623
6	83.25	85	40	627.25	629
7	175.25	177	41	633.25	635
8	181.25	183	42	639.25	641
9	187.25	189	43	645.25	647
10	193.25	195	44	651.25	653
11	199.25	201	45	657.25	659
12	205.25	207	46	663.25	665
13	211.25	213	47	669.25	671
14	471.25	473	48	675.25	677
15	477.25	479	49	681.25	683
16	483.25	485	50	687.25	689
17	489.25	491	51	693.25	695
18	495.25	497	52	699.25	701
19	501.25	503	53	705.25	707
20	507.25	509	54	711.25	713
21	513.25	515	55	717.25	719
22	519.25	521	56	723.25	725
23	525.25	527	57	729.25	731
24	531.25	533	58	735.25	737
25	537.25	539	59	741.25	743
26	543.25	545	60	747.25	749
27	549.25	551	61	753.25	755





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28	555.25	557	62	759.25	761
29	561.25	563	63	765.25	767
30	567.25	569	64	771.25	773
31	573.25	575	65	777.25	779
32	579.25	581	66	783.25	785
33	585.25	587	67	789.25	791
34	591.25	593	68	795.25	797
35	597.25	599	69	801.25	803

## 16. US Cable TV Channel Frequencies

### 16.1 Standard TV Channel

Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)	Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)
2	55.25	57	64	463.25	465
3	61.25	63	65	469.25	471
4	67.25	69	66	475.25	477
1	-	-	67	481.25	483
5	77.25	79	68	487.25	489
6	83.25	85	69	493.25	495
95	91.25	93	70	499.25	501
96	97.25	99	71	505.25	507
97	103.25	105	72	511.25	513
98	109.25	111	73	517.25	519
99	115.25	117	74	523.25	525
14	121.25	123	75	529.25	531
15	127.25	129	76	535.25	537
16	133.25	135	77	541.25	543
17	139.25	141	78	547.25	549
18	145.25	147	79	553.25	555
19	151.25	153	80	559.25	561



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20	157.25	159	81	565.25	567
21	163.25	165	82	571.25	573
22	169.25	171	83	577.25	579
7	175.25	177	84	583.25	585
8	181.25	183	85	589.25	591
9	187.25	189	86	595.25	597
10	193.25	195	87	601.25	603
11	199.25	201	88	607.25	609
12	205.25	207	89	613.25	615
13	211.25	213	90	619.25	621
23	217.25	219	91	625.25	627
24	223.25	225	92	631.25	633
25	229.25	231	93	637.25	639
26	235.25	237	94	643.25	645
27	241.25	243	100	649.25	651
28	247.25	249	101	655.25	657
29	253.25	255	102	661.25	663
30	259.25	261	103	667.25	669
31	265.25	267	104	673.25	675
32	271.25	273	105	679.25	681
33	277.25	279	106	685.25	687
34	283.25	285	107	691.25	693
35	289.25	291	108	697.25	699
36	295.25	297	109	703.25	705
37	301.25	303	110	709.25	711
38	307.25	309	111	715.25	717
39	313.25	315	112	721.25	723
40	319.25	321	113	727.25	729
41	325.25	327	114	733.25	735
42	331.25	333	115	739.25	741
43	337.25	339	116	745.25	747
44	343.25	345	117	751.25	753
45	349.25	351	118	757.25	759
46	355.25	357	119	763.25	765
47	361.25	363	120	769.25	771
48	367.25	369	121	775.25	777
49	373.25	375	122	781.25	783



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50	379.25	381	123	787.25	789
51	385.25	387	124	793.25	795
52	391.25	393	125	799.25	801
53	397.25	399	126	805.25	807
54	403.25	405	127	811.25	813
55	409.25	411	128	817.25	819
56	415.25	417	129	823.25	825
57	421.25	423	130	829.25	831
58	427.25	429	131	835.25	837
59	433.25	435	132	841.25	843
60	439.25	441	133	847.25	849
61	445.25	447	134	853.25	855
62	451.25	453	135	859.25	861
63	457.25	459			

### 16.2 IRC TV Channel

Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)	Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)
2	55.25	57	64	463.25	465
3	61.25	63	65	469.25	471
4	67.25	69	66	475.25	477
5	73.25	75	67	481.25	483
6	79.25	81	68	487.25	489
7	85.25	87	69	493.25	495
8	91.25	93	70	499.25	501
9	97.25	99	71	505.25	507
10	103.25	105	72	511.25	513
11	—	—	73	517.25	519
12	—	—	74	523.25	525
13	121.15	122.9	75	529.25	531



## MT537x Application Note

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15	127.15	128.9	76	535.25	537
16	133.15	134.9	77	541.25	543
17	139.15	140.9	78	547.25	549
18	145.15	146.9	79	553.25	555
19	151.15	152.9	80	559.25	561
20	157.15	158.9	81	565.25	567
21	163.15	164.9	82	571.25	573
22	169.15	170.9	83	577.25	579
7	175.25	177	84	583.25	585
8	181.25	183	85	589.25	591
9	187.25	189	86	595.25	597
10	193.25	195	87	601.25	603
11	199.25	201	88	607.25	609
12	205.25	207	89	613.25	615
13	211.25	213	90	619.25	621
23	217.25	219	91	625.25	627
24	223.25	225	92	631.25	633
25	229.25	231	93	637.25	639
26	235.25	237	94	643.25	645
27	241.25	243	100	649.25	651
28	247.25	249	101	655.25	657
29	253.25	255	102	661.25	663
30	259.25	261	103	667.25	669
31	265.25	267	104	673.25	675
32	271.25	273	105	679.25	681
33	277.25	279	106	685.25	687
34	283.25	285	107	691.25	693
35	289.25	291	108	697.25	699
36	295.25	297	109	703.25	705
37	301.25	303	110	709.25	711
38	307.25	309	111	715.25	717
39	313.25	315	112	721.25	723
40	319.25	321	113	727.25	729
41	325.25	327	114	733.25	735



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42	-	-	115	739.25	741
43	337.25	339	116	745.25	747
44	343.25	345	117	751.25	753
45	349.25	351	118	757.25	759
46	355.25	357	119	763.25	765
47	361.25	363	120	769.25	771
48	367.25	369	121	775.25	777
49	373.25	375	122	781.25	783
50	379.25	381	123	787.25	789
51	385.25	387	124	793.25	795
52	391.25	393	125	799.25	801
53	397.25	399	126	805.25	807
54	403.25	405	127	811.25	813
55	409.25	411	128	817.25	819
56	415.25	417	129	823.25	825
57	421.25	423	130	829.25	831
58	427.25	429	131	835.25	837
59	433.25	435	132	841.25	843
60	439.25	441	133	847.25	849
61	445.25	447	134	853.25	855
62	451.25	453	135	859.25	861
63	457.25	459			

### 16.3 HRC TV Channel

US Cable TV HRC Channel Frequencies					
Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)	Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)
2	54	55.75	64	462	463.75
3	60	61.75	65	468	469.75



MT537x Application Note

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4	66	67.75	66	474	475.75
1	72	73.75	67	480	481.75
5	78	79.75	68	486	487.75
6	84	85.75	69	492	493.75
95	90	91.75	70	498	499.75
96	96	97.75	71	504	505.75
97	102	103.75	72	510	511.75
98	--	--	73	516	517.75
99	--	--	74	522	523.75
14	120	121.75	75	528	529.75
15	126	127.75	76	534	535.75
16	132	133.75	77	540	541.75
17	138	139.75	78	546	547.75
18	144	145.75	79	552	553.75
19	150	151.75	80	558	559.75
20	156	157.75	81	564	565.75
21	162	163.75	82	570	571.75
22	168	169.75	83	576	577.75
7	174	175.75	84	582	583.75
8	180	181.75	85	588	589.75
9	186	187.75	86	594	595.75
10	192	193.75	87	600	601.75
11	198	199.75	88	606	607.75
12	204	205.75	89	612	613.75
13	210	211.75	90	618	619.75
23	216	217.75	91	624	625.75
24	222	223.75	92	630	631.75
25	228	229.75	93	636	637.75
26	234	235.75	94	642	643.75
27	240	241.75	100	648	649.75
28	246	247.75	101	654	655.75
29	252	253.75	102	660	661.75
30	258	259.75	103	666	667.75
31	264	265.75	104	672	673.75



Confidential

Specifications are subject to change without notice

32	270	271.75	105	678	679.75
33	276	277.75	106	684	685.75
34	282	283.75	107	690	691.75
35	288	289.75	108	696	697.75
36	294	295.75	109	702	703.75
37	300	301.75	110	708	709.75
38	306	307.75	111	714	715.75
39	312	313.75	112	720	721.75
40	318	319.75	113	726	727.75
41	324	325.75	114	732	733.75
42	330	331.75	115	738	739.75
43	336	337.75	116	744	745.75
44	342	343.75	117	750	751.75
45	348	349.75	118	756	757.75
46	354	355.75	119	762	763.75
47	360	361.75	120	768	769.75
48	366	367.75	121	774	775.75
49	372	373.75	122	780	781.75
50	378	379.75	123	786	787.75
51	384	385.75	124	792	793.75
52	390	391.75	125	798	799.75
53	396	397.75	126	804	805.75
54	402	403.75	127	810	811.75
55	408	409.75	128	816	817.75
56	414	415.75	129	822	823.75
57	420	421.75	130	828	829.75
58	426	427.75	131	834	835.75
59	432	433.75	132	840	841.75
60	438	439.75	133	846	847.75
61	444	445.75	134	852	853.75
62	450	451.75	135	858	859.75
63	456	457.75			

# MT5112BD

## Preliminary Datasheet

- FEATURES
- GENERAL DESCRIPTION
- FUNCTIONAL BLOCK DIAGRAM
- PIN ASSIGNMENT
- PIN DESCRIPTION
- TIMING INFORMATION
- ELECTRICAL CHARACTERISTICS
- OUTLINE DIMENSION & TOP MARKING



## FEATURES

- ✦ Compliant with ATSC digital television standard
- ✦ Supports SCTE DVS-031 and ITU J.83 Annex B digital CATV standard
- ✦ Accepts direct IF (44 MHz or 43.75MHz) and low IF (5.38MHz)
- ✦ Differential IF input with programmable input signal level: 0.5Vpp to 2Vpp
- ✦ NTSC interference rejection capability
- ✦ Compensate echo up to -35 to +60 $\mu$ s range for terrestrial HDTV reception
- ✦ Pass all Brazil fading channel ensembles
- ✦ Meet all ATSC/A74 requirement
- ✦ On-chip programmable gain amplifier
- ✦ 25MHz crystal for clock generation
- ✦ Excellent adjacent and co-channel rejection capability, only single SAW is required
- ✦ Full-digital timing recovery, no VCXO is required
- ✦ Full-digital frequency offset recovery with wide acquisition range  $\pm 1$ MHz for ATSC and  $\pm 250$ kHz for CATV reception
- ✦ Dual digital AGC controls for IF and RF respectively
- ✦ MPEG-2 transport stream output in parallel or serial format
- ✦ On-chip error rate estimators for TS packets, TCM decoder, and equalizer
- ✦ EIA/CEA-909 antenna interface, both mode A and mode B are supported
- ✦ Controlled by I<sup>2</sup>C interface
- ✦ Supports sleep mode to save power consumption
- ✦ Core power supply: 1.8V, peripheral power supply: 3.3V
- ✦ 100-TQFP with lead free package

## GENERAL DESCRIPTION

D TV  
The MT5112BD is a highly integrated single-chip for digital terrestrial HDTV and digital cable TV demodulation. The chip is designed specifically for the digital terrestrial HDTV and CATV receivers, and is fully compliant with ATSC A/53, SCTE DVS-031, and ITU J.83 Annex B standards.

### 8-VSB and Clear-QAM Reception

MT5112BD contains a 10-bit A/D converter, an 8-VSB/QAM demodulator, followed by a trellis-coded modulation (TCM) decoder and a Reed-Solomon forward error correction (FEC) decoder. Moreover, an embedded 8-bit microprocessor intelligently handles the acquisition and tracking to ensure the best receiving performance under various channel conditions. The microprocessor communicates with the external host controller via an I<sup>2</sup>C-compatible interface, and also provides direct control to the RF tuner via another I<sup>2</sup>C-compatible interface.

MT5112BD accepts the tuner IF output centered at 44MHz or 43.75MHz, or the low IF signals from a down-converter. With good adjacent channel immunity, additional IF SAW filters for adjacent channel rejection can be saved. An on-chip programmable gain-controlled amplifier (PGA) is designed to provide extra signal gain when the tuner output level is low. The amplified IF signal is then sample and digitized for further demodulation process.

MT5112BD keeps A/D input power level at a desired level so as to maximize the received SNR. It measures the power level of the digitized samples and provide two signals (both sigma-delta encoded; one delayed and one non-delayed) for front-end gain control purpose. The signals is low-pass filtered before connected to tuner or IF gain stages.

For the 8-VSB reception, the carrier frequency offset is estimated and compensated by a fully digital synchronizer. It also controls the rate conversion in the digital re-sampling device by estimating the sampling frequency offset; hence no external VCXO is required. The digital synchronizer simultaneously offers very wide frequency acquisition range and stable tracking capability. This makes MT5112BD robust

work under severe impairment conditions.

The MT5112BD is equipped with a powerful equalizer for mitigating the multi-path effects due to terrestrial propagation of 8-VSB signals. The delicate equalizer design makes the MT5112BD boast its ability for strong echo cancellation. With this powerful equalizer, the MT5112BD can not only easily pass the tests of A74 equalization mask, ATTC channel ensembles, CRC channel ensembles, but also provide superior capability of live signal receptions.

For cable signal reception, the MT5112BD adopts the fully digital modules for timing and carrier synchronization, with no external VCXO required. Specially designed carrier synchronization module enables the MT5112BD passing the OpenCable ATP burst and phase noise tests, while maintaining excellent reception performance under normal reception conditions.

The MT5112BD also utilizes a powerful equalizer for performing channel equalization in cable environments. The MT5112BD equipped with this powerful equalizer can easily pass the SCTE channel tests and offer stable and excellent live signal receptions.

The following FEC decoder corrects most of the errors by the concatenation of the TCM and Reed-Solomon decoders with an in-between de-interleaver. Specifically for the digital cable TV reception, the MT5112BD first detects and aligns de-puncturing timing of the received sequence before TCM decoding. Besides, two synchronization circuits are each inserted before the de-interleaver and after the Reed-Solomon decoder to automatically delineate the FEC frames and transport stream packets respectively. An on-chip error rate estimator can simultaneously monitor the receiving qualities at the three stages: the equalizer output, the TCM decoder, and the transport stream packets. At the last stage, the MT5112BD incorporates a buffer to smooth out the uneven arrival time of transport stream packets. The chip finally outputs the smoothed decoded MPEG-2 transport stream packets in either the serial or parallel transport stream format.

In addition to the demodulation of HDTV signal, MT5112BD provides the capability to remove narrow-band interference such as the co-channel NTSC signal and CW tones which generally exists in

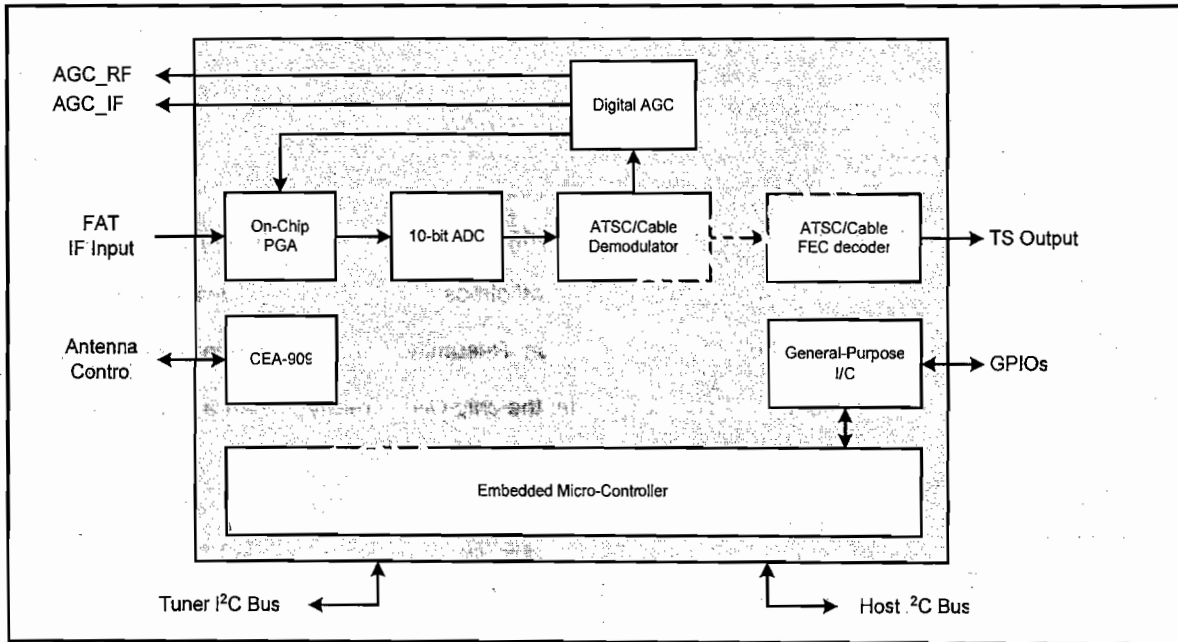
broadcast environment.

To achieve the best reception, an antenna control interface compliant with EIA/CEA-909 is equipped into the MT5112BD to configure the antenna parameters. Both the unidirectional mode A and the bi-directional mode B operation schemes are supported.

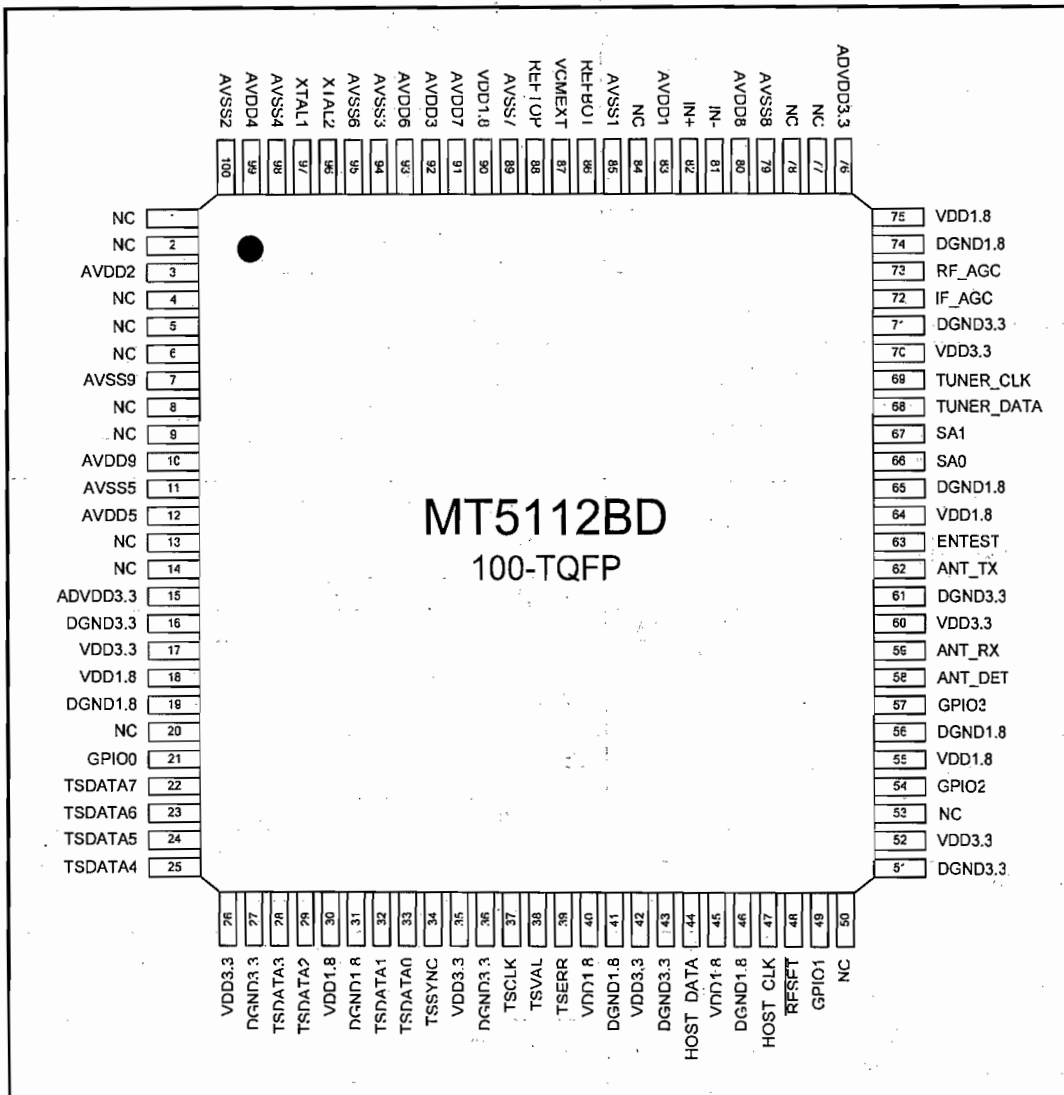
### **Power Saving Mode**

The MT5112BD is designed with efficient mechanisms of power saving. When configured to enter the sleep mode by the system host, it can immediately turn off almost all embedded hardware except the on-chip microprocessor to reduce the power consumption. Resuming from sleep mode is also triggered by the system host. Upon returning to the operation mode, the chip will be ready to start a new acquisition.

## FUNCTIONAL BLOCK DIAGRAM



**PIN ASSIGNMENT**



## PIN DESCRIPTION

### For FAT Applications

Pin Numbers	Symbol	Type	Description
<b>Transport Stream</b>			
22, 23, 24, 25, 28, 29, 32, 33	TSDATA[7:0]	O	TS data output
34	TSSYNC	O	TS packet start signal
38	TSVAL	O	TS output valid signal
37	TSCLK	O	TS output clock
39	TSERR	O	TS packet error indicator
<b>Analog Signal</b>			
82	IN+	I	Analog differential IF input
81	IN-	I	
88	REFTOP	O	ADC reference top voltage. Decouple with a capacitor to AVSS
86	REFBOT	O	ADC reference bottom voltage. Decouple with a capacitor to AVSS
87	VCMEXT	O	ADC common mode voltage
<b>Antenna Interface</b>			
62	ANT_TX	O	CEA-909 antenna control: transmit data
58	ANT_DET	I	CEA-909 antenna control: detection signal
59	ANT_RX	I	CEA-909 antenna control: receive data
<b>Clock Generation</b>			
97	XTAL1	I	25MHz crystal input
96	XTAL2	I	
<b>Control Signals</b>			
47	HOST_CLK	I	Host processor serial clock input, 5 volt compatible
44	HOST_DATA	I/O	Host processor serial data pin, 5 volt compatible
69	TUNER_CLK	O	Tuner serial clock output, 5 volt compatible
68	TUNER_DATA	I/O	Tuner serial data pin, 5 volt compatible
72	IF_AGC	O	IF AGC output
73	RF_AGC	O	RF AGC output
48	RESET	I	Power reset pin, low active
66	SA0	I	Chip slave address selection pin, tie to VDD3.3 or DGND
67	SA1	I	Chip slave address selection pin, tie to VDD3.3 or DGND
<b>Power Supply</b>			
17, 26, 35, 42, 52, 60, 70	VDD3.3	P	Digital power supply, tie to 3.3V
18, 30, 40, 45, 55, 64, 75	VDD1.8	P	Digital power supply, tie to 1.8V
16, 19, 27, 31, 36, 41, 43, 46, 51, 56, 61, 63, 65, 71, 74	DGND	P	Digital ground, tie to digital ground plane
3, 10, 12, 80, 83, 91, 92, 93, 99	AVDD	P	Analog power supply, tie to 3.3V
7, 11, 79, 85, 89, 94, 95, 98, 100	AVSS	P	Analog ground, tie to analog ground plane
15, 76	ADVDD3.3	P	Digital power supply for analog component, tie to 3.3V
90	AVDD1.8	P	Digital power supply for analog component, tie to 1.8V
<b>General-Purpose I/O</b>			
57, 54, 49, 21	GPIO[3:0]	I/O	General-Purpose I/Os

## 24-bit, 192 KHz. CODEC: 6 Ch DAC, 5 Input Mux Stereo ADC

### DESCRIPTION

The CE2836 is a mixed signal CMOS monolithic audio Codec. It contains six multi-bit sigma delta DAC and a stereo ADC with 5 input multiplexer, Ideal for audio playback and recording applications.

The DAC consists of 128-time interpolation filters, 3<sup>rd</sup> order multi-bit  $\Sigma\Delta$  modulators, switch capacitors and analog reconstruction filters. The  $\Sigma\Delta$  converter offers superior differential linearity, with minimum distortion due to component mis-match. high tolerance to clock jitter. Additionally it includes separated digital volume control for each channel.

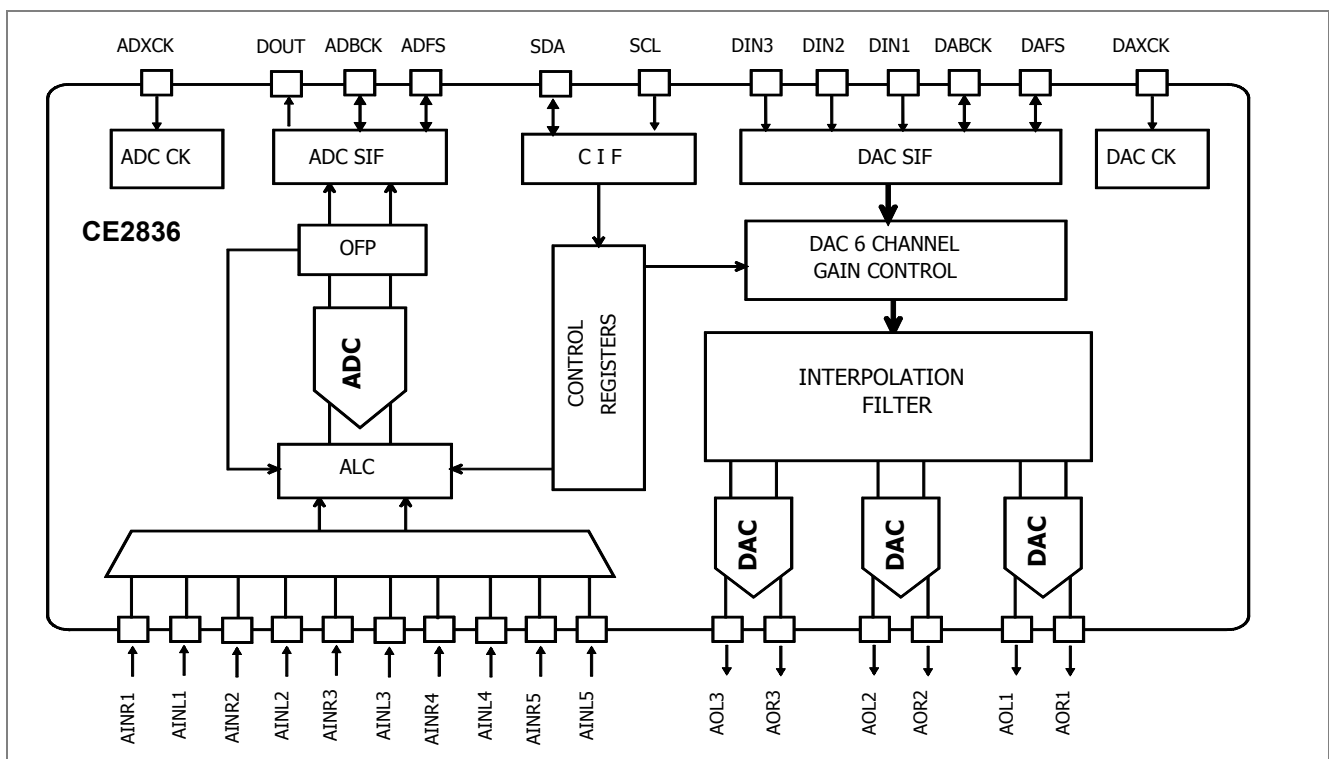
The ADC utilizes cascaded  $\Sigma\Delta$  architecture. The internal digital filter has a 20K bandwidth. It support sampling frequency up to 96K Hz. The ADC also includes a analog Automatic Level Control and Noise Gate function to ease the recording applications.

### FEATURES

- Six Channel Audio DAC.
  - 104 dB SNR (A Weighted).
  - -82 dB THD + N Ratio (A Weighted).
  - 32K - 192 KHz. Sampling Rates.
  - On -chip Reconstruction Filters.
  - Independent Digital Volume Control.
- Stereo Audio ADC.
  - 5 Channel ADC inputs.
  - Up to 96K Sampling Rate.
  - With Automatic Level Control and Noise Gate.
  - Includes ALC and Noise Gate Functions.
- I<sup>2</sup>S, Left and Right Justified Digital I/F Formats.
- 2-wire Serial Control Interface.
- 3.3 Volt Power Supply.

### Applications

- Digital Surround Sound For Home Theatre
- DVD or DVD Recordable.





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**CE2836 Performance**

<b>Item</b>	<b>DAC PERFORMANCE SPECIFICATIONS</b>	<b>Spec.</b>
1	Audio Output Level	1 Vrms
2	Audio Bandwidth 20Hz - 20 KHz	+/- 0.1 dB
3	SNR (A-weight)	>104 dB
4	THD + NOISE (A-weight, 0 dB input)	< -82 dB
5	Dynamic Range	94 dB
6	Channel Separation	< -92 dB
7	Nonlinear Distortion	< 0.25 dB
8	Channel Gain Error	< 0.1 dB
	<b>ADC PERFORMANCE SPECIFICATIONS</b>	
1	Maximum Input Level	4 Vpp
2	0 dB Audio Input Level	1 Vrms
3	Audio Bandwidth 20Hz - 20 KHz	+/- 0.5 dB
4	SNR (A-weight)	>98 dB
5	THD + NOISE (A-weight, 0 dB input)	< -88 dB
6	Dynamic Range	94 dB
7	Channel Separation	< -96 dB
8	Nonlinear Distortion	< 0.25 dB
9	Channel Gain Error	< 0.5 dB

All Measurement were taken with only one channel active.

**Description (continue)**

The DAC support conversion rate from 32K to 192KHz while the ADC from 32K to 96K. The CE2836 support 32, 24, 20 and 16-bit input data. It also support multiple sampling frequency data. Each DAC has its own individual volume control.

**XCK REQUIREMENT**

The CE2836 supports 32K, 44.1K, 48K, 96K and 192K sampled audio in DAC operations and 32K, 44.1K, 48K and 96K sampled audio in ADC operations. The oversampled clock, XCK, requirements are listed in Table 1 and 2.

The DAC and ADC PCM serial port can be configured as ‘Master’ or ‘Slave’ independently and each has separated over sampling clock input. In the ‘Slave Mode’ PCM serial port operation if the AUTODEC, CR1[7]==1, there is an clock frequency detection circuit to set up the system clock, the users don’t need to set the SRC registers. However in the ‘master mode’ operation the users need to set the SRC registers for the serial audio clock generations

**Table 1.**

Sampling Rate	DAC XCK Requirement				
		DACDIV==0		DACDIV==1	
32 K	XCK Freq	12.288 MHz	8.192 Mhz.	24.576 Mhz	16.384 Mhz
	SRC[1:0]	[11], 384 fs	(#), 256 fs	[11], 768fs	(#), 512 fs
44.1K	XCK Freq	16.934 Mhz	11.29 Mhz.	33.869 Mhz	22.579 Mhz
	SRC[1:0]	[11], 384fs	[10], 256 fs	[11], 768 fs	[10], 512fs
48 K	XCK Freq	18.432 MHz	12.288 Mhz	36.864 MHz	24.576 Mhz.
	SRC[1:0]	[11], 384 fs	[10], 256 fs	[11], 768fs	[10], 512 fs
96 K	XCK Freq	18.432 MHz	12.288 Mhz.	36.864 MHz	24.576 Mhz.
	SRC[1:0]	[01], 192 fs	[00], 128 fs	[01], 384 fs	[00], 256 fs
192 K	XCK Freq	18.432 Mhz	12.288 Mhz.	36.864 MHz	24.576 Mhz.
	SRC	(#), 96 fs	(#), 64 fs	(#), 192 fs	(#), 128 fs

All the XCK clock rate listed are supported in the ‘Slave Mode’  
 SRC Registers are used in the ‘Master Mode’. (#) are not supported in the in the ‘Master Mode’ .  
 DAC AUTODET is CREG1[7], DAC SRC[1:0]are CREG1[6:5] and DACDIV is CREG1[4].

Table 2.

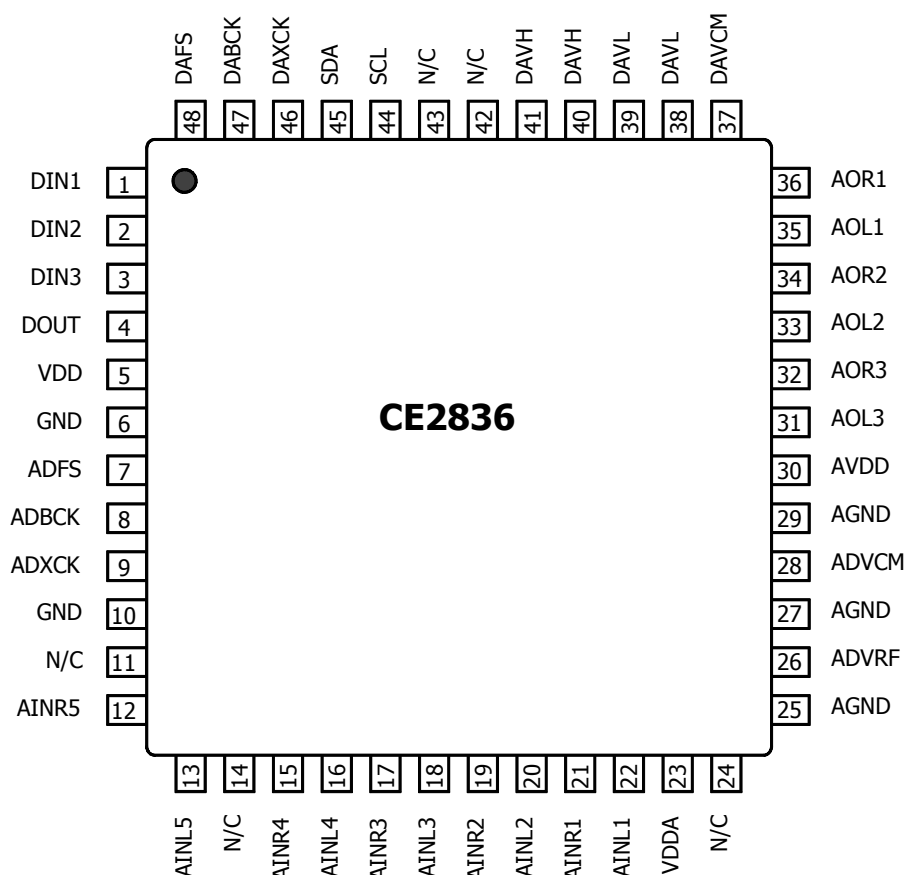
Sampling Rate	ADC XCK Requirement				
		DACDIV==0		DACDIV==1	
32 K	XCK Freq	12.288 MHz	8.192 Mhz.	24.576 Mhz	16.384 Mhz
	SRC[1:0]	[10], 384 fs	(#), 256 fs	[10], 768fs	(#), 512 fs
44.1K	XCK Freq	16.934 Mhz	11.29 Mhz.	33.869 Mhz	22.579 Mhz
	SRC[1:0]	[10], 384fs	[00], 256 fs	[10], 768 fs	[00], 512fs
48 K	XCK Freq	18.432 MHz	12.288 Mhz	36.864 MHz	24.576 Mhz.
	SRC[1:0]	[10], 384 fs	[00], 256 fs	[10], 768fs	[00], 512 fs
96 K	XCK Freq	18.432 MHz	12.288 Mhz.	36.864 MHz	24.576 Mhz.
	SRC[1:0]	[11], 192 fs	[01], 128 fs	[11], 384 fs	[01], 256 fs

All the XCK clock rate listed are supported in the 'Slave Mode' .

SRC Registers are used in the '*Master Mode*'. (#) are not supported in the 'Master Mode' .

ADC AUTODET is CREG9[7], DAC SRC[1:0] are CREG9[6:5] and DACDIV is CREG9[4].

## PIN ASSIGNMENT



## PIN DESCRIPTION

Pin Name	Pin #	Type	Description
<b>DIGITAL</b>			
N/C	43		No connection. It can be tied to GND.
SDA	44	I/O	Serial command port data line.
SCL	45	I	Serial command port clock line.
DAXCK	46	I	External master clock input for DAC.
DABCK	47	I	DAC audio serial data clock Input pin (default) if DAC I/F is configured to be 'slave' else it is an Output.
DAFS	48	I	DAC left/right channel clock pin. Please refer to Figure 1 PCM data format for its definition Input (default) if DAC I/F is configured to be 'slave' else it is an output
DIN1	1	I	DAC Channel 1 or TDM serial audio data input.
DIN2	2	I	DAC Channel 2 serial audio data input.

**PIN DESCRIPTION (Continued)**

Pin Name	Pin #	Type	Description
DIN3	3	I	DAC Channel 3 serial audio data input.
DOUT	4	O	Serial ADC output
VDD	5	+3.3V	Digital power supply, 3.3 Volt.
GND	6	GND	Digital ground
ADFS	7	I/O	ADC left/right channel clock pin. Please refer to Figure 1 PCM data format for its definition. Input (default) if ADC I/F is configured to be 'slave' else it is an output
ADBACK	8	I/O	External master clock input for ADC. Input (default) if ADC I/F is configured to be 'slave' else it is an output
ADXCK	9	I	ADC audio serial data clock input.
<b>GND</b>	10	I	Digital ground

**Analog**

N/C	11		No connection. It can be tied to AGND.
AINR5	12	I	ADC channel 5 right input. Input resistance is 20K Ohm
AINL5	13	I	ADC channel 5 left input. Input resistance is 20K Ohm
N/C	14		No connection. It can be tied to AGND.
AINR4	15	I	ADC channel 4 right input. Input resistance is 20K Ohm
AINL4	16	I	ADC channel 4 left input. Input resistance is 20K Ohm
AINR3	17	I	ADC channel 3 right input. Input resistance is 20K Ohm
AINL3	18	I	ADC channel 3 left input. Input resistance is 20K Ohm
AINR2	19	I	ADC channel 2 right input. Input resistance is 20K Ohm
AINL2	20	I	ADC channel 2 left input. Input resistance is 20K Ohm
AINR1	21	I	ADC channel 1 right input. Input resistance is 20K Ohm
AINL1	22	I	ADC channel 1 left input. Input resistance is 20K Ohm
AVDD	23	+3.3V	ADC power supply.
N/C	24		No connection. It can be tied to AGND.
AGND	25	GND	Analog ground pin.
ADVRF	26	O	ADC reference voltage. It should be decoupled to AGND with a 22 uF capacitor in parallel with a 0.1 uF. Its value should be AVDD/2 volt.
AGND	27	GND	Analog ground pin.

**PIN DESCRIPTION (Continued)**

Pin Name	Pin #	Type	Description
ADVCM	28	O	ADC comment mode voltage. It should be decoupled to AGND with a 22 uF in parallel with a 0.1 uF. Signal level is AVDD/2.
AGND	29	GND	Analog ground pin.
AVDD	30	+3.3V	DAC power supply.
AOL3	31	O	Analog left channel 3 output
AOR3	32	O	Analog right channel 3 output
AOL2	33	O	Analog left channel 2 output
AOR3	34	O	Analog right channel 2 output
AOL1	35	O	Analog left channel 1 output
AOR1	36	O	Analog right channel 1 output
DAVCM	37	O	DAC comment mode voltage. It should be connected to a 22 uF in parallel with a 0.1 uF decoupling capacitors to ground. Signal level is AVDD/2.
DAVL	38, 39	GND	DAC negative reference voltage. It should be tied to AGND.
DAVH	40,41	I	DAC positive reference voltage. It should be connected to AVDD via a 180 ohm serial resistor, and a 22 uF in parallel with a 0.1 uF decoupling capacitors to ground.
N/C	42		No connection. It can be tied to AGND.

## DIGITAL AUDIO SERIAL INTERFACE

There are two independent PCM serial ports, one for DAC and one for ADC. The DAC digital serial interface consists of 3 serial input pins, DIN1, DIN2, DIN3, one serial clock input/output pin, DABCK, and one left/right indicator input/output pin, DAFS. The ADC consists of a data output pin, DOUT and one serial clock input/output pin, ADBCK, and one left/right indicator input/output pin, ADFS. The BCK and FS are output pins when the respective port is configured as 'Master', and input pin when it is configured as 'Slave' port. The Master/Slave operations are setup via CREGA[7] and CREGA[3]. The data are 2's complement MSB first numbers. The CE2836 supports four resolution, which are selected programming the control register CREG0 and CRFEGA via the I<sup>2</sup>C serial control port. Table 3 describes these four resolution.

**Table (3): Audio Serial Data Input Resolution,**

Format	NBIT[1:0]	DIN, DOUT
0	00	16-bit
1	01	20-bit
2	10	24-bit (default)
3	11	32-bit

The DIN and DOUT can be either 24-bit or 32-bit per frame as well as left justified, right justified or I2S. .

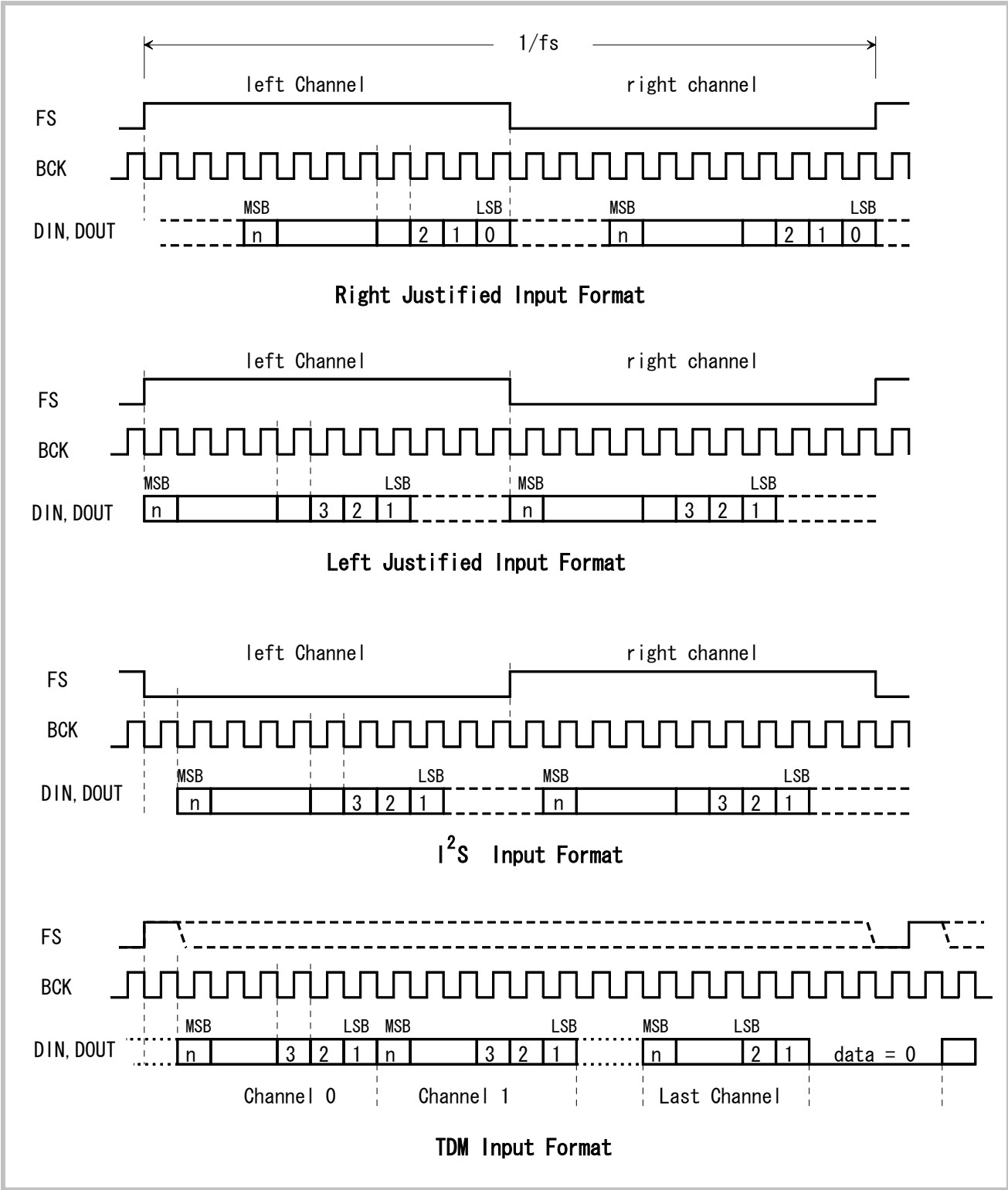
**Table (4): Audio Serial Data Input Modes**

Mode	FMT[1:0]	DIN, DOUT
0	00	Right Justified
1	01	Left Justified
2	10	I2S (default)
3	11	TDM

### TDM Input Format

The CE2836 support Time Division Multiplex data input. In this format only one data input pin is required. The six channel data are sent in serial order, channel 1 first, followed by channel 2 and so forth. The number of bits per channel is defined by CREG0[5:4].

Figure 1. Audio Serial Input Data Format





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## DAC INFINITE ZERO DETECTION

The CE2836 DAC has an Infinite Zero Detection circuit which detects zero in the Audio Serial Port that lasts for approximately 0.2 sec. By default, the zero detection circuit is on.

## DAC Digital Attenuation

Each DAC contains an Digital Attenuation block. The attenuation values are hold in the Volume Control Registers. The Value 80H corresponds to Full Scale, 0dB. and each decrement correspond to -0.5 dB additional attenuation.

## ADC Gain and ALC

Each channel of ADC input includes a Analog Gain. The Gain is controlled by CREGC, ADC Gain Selection, The gain range is from +6 dB to -9 dB. with 1 dB step. The GAIN = 9 corresponds to 0dB gain. The AUTOMATIC LEVEL CONTROL set the ADC maximum digital output to a prescribed value by automatic manipulating the analog gain. The ALC is controlled by CREG8, ADC PROC. REGISTER..

**Table (5): ALC Target Level**

ALC[2:0]	Maximum Digital Output
000	-1 dB FS
001	-2 dB FS
010	-3 dB FS
011	-4 dB FS
100	-5 dB FS
101	-6 dB FS
110	-7 dB FS
111	-8 dB FS

**Table (6): ALC Hold Time**

ALCHTM	Hold Time	Comment
0	340 msec.	For music program
1	5.3 msec	For speech program

### ADC Noise Gate

Noise Gate remove hissing noise during silence period. It is useful for recording noisy program. While Noise Gate is enabled the ADC digital output will be zeroed if the signal level below a predetermined value for about 0.5 seconds. The noise Gate is controlled by the same ADC PROC. REGISTER.

**Table (7): Noise Gate Threshold**

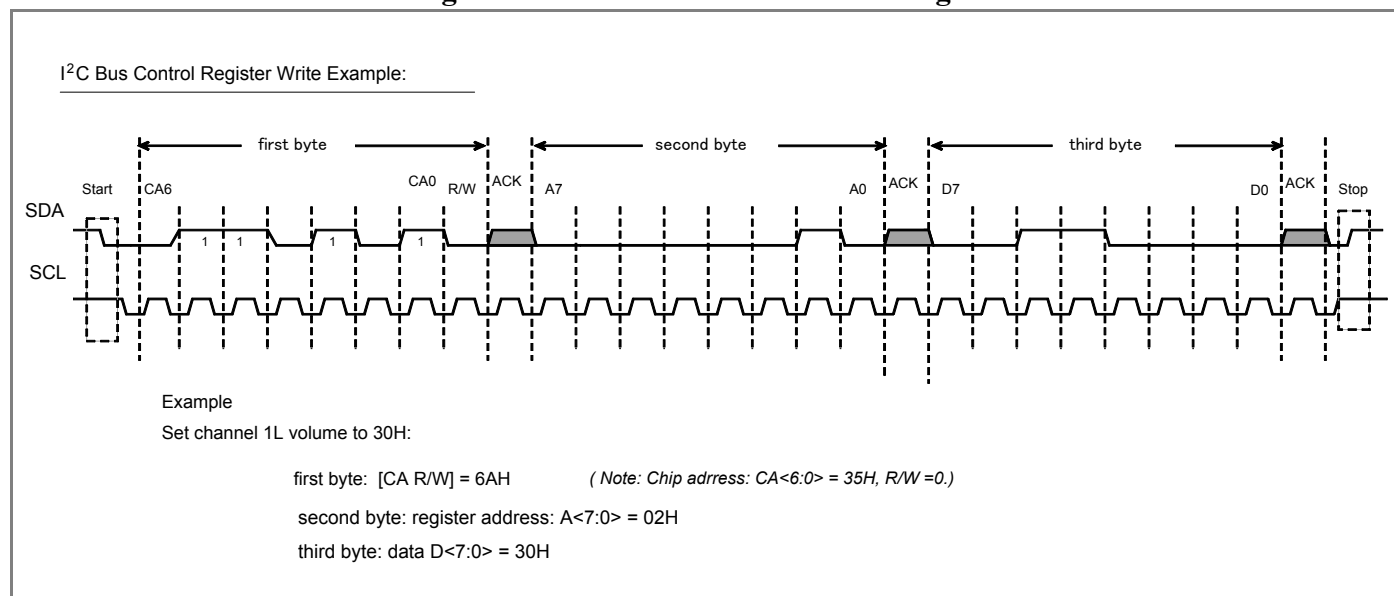
NGTH[1:0]	Threshold
00	-66 dB
01	-72 dB
10	-78 dB
11	-84 dB

### Serial Command Port

The user can select the chip operation mode by programming the internal control registers through serial I<sup>2</sup>C port. The Chip Address for the CE2836 is 35H. The protocol for write operation consists of sending 3 byte data to CE2836, following each byte is the acknowledges generated by CE2836. The first byte is the 7-bit Chip Address followed by the read/write bit (read is high, write is low). The second byte is the control register address. The third byte is the control register data.

Upon power up, all programmable registers are set to default values. Figure 2 describes the serial command port timing relationship.

**Figure 2. Serial Command Port Timing**



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**SERIAL PORT CONTROL REGISTER ASSIGNMENT**

There are 8 registers dedicated to the CE2836 for chip functional programming, The register addresses assignments are

Address (decimal)	Register	Default Value	Register Function
0	CREG0[7:0]	A0	DAC Control REG0: Data input format, de-emphasis filter selection
1	CREG1[7:0]	80	DAC Control REG1: Input format and PLL output frequency selection
2	CREG2[7:0]	80	Volume Control Register for DAC channel 1, left
3	CREG3[7:0]	80	Volume Control Register for DAC channel 1, right
4	CREG4[7:0]	80	Volume Control Registerl for DAC channel 2, left
5	CREG5[7:0]	80	Volume Control Register for DAC channel 2, right
6	CREG6[7:0]	80	Volume Control Register for DAC channel 3, left
7	CREG7[7:0]	80	Volume Control Registerl for DAC channel 3, right
8	CREG8[7:0]	82	ADC Proc REG: ALC and Noise Gate Control Registers
9	CREG9[7:0]	A0	ADC Control Register.
10	CREGA[7:0]	00	CHIP Control Register.
11	CREGB[7:0]	01	ADC MUX Select.
12	CREGC[7:0]	99	ADC Input Gain Select
13	CREGD[7:0]	92	Chip Soft Reset.

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**CONTROL REGISTERS DESCRIPTION**
**CREG0, DAC Control Register 0 (ADRS=hex00, default=hexA0)**

ADDR[3:0]	CREG0[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 00	FMT[1:0]		NBIT[1:0]		AMUTE	DEEMP	FSMPL[1:0]	
Default Value	1	0	1	0	0	0	0	0

FMT[1:0] Digital Serial Bus Format Select

00: - Normal or Right Justified Format.

01: -Left Justified Format.

10: - I2S Format.(default)

11: - TDM, Multi-channel Time Division Multiplex Format

NBIT[1:0]: - These two bits define the serial audio input resolution for right justified and TDM mode

00: - 16-bit resolution.

01: - 20-bit resolution.

10: - 24-bit resolution (default).

11: - 32-bit resolution.

AMUTE: - Auto-mute detection enable.

0: - Auto-mute enabled. (default)

1: - No auto-mute.

DEEMP: - Enable de-emphasis

0: - Normal. (default)

1: - enable de-emphasis.

FSMPL: - Interpolation filter selection.

These two bits are recognized only when "AUTODET" bit of the CREG1 is set to '0'.

0X: - 44.1 or 48K sampling.(default)

10: - 96K sampling.

11: - 192K sampling.

**CREG1, DAC Control Register 1(ADRS=hex01, default=hex80)**

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 01	AUTODET	SRC[1:0]		CKDIV2	X	MUTE56	MUTE34	MUTE12
Default Value	1	0	0	0	0	0	0	0

AUTODET Automatically detects the serial audio input data sampling rate clock frequency.

0: - do not use auto-detect

1: - automatically detects the serial audio input data sampling rate and clock frequency.

SRC[1:0]: - DAC Sampling Rate Selection. It is used in the DAC Master Mode, CRA[7]=1, to generate DAFS and DABCK.

00: - Sampling Rate = XCK/128.

01: - Sampling Rate = XCK/192.

10: - Sampling Rate = XCK/256.

11: - Sampling Rate = XCK/384.

CKDIV2: - Enable the ADXCK Clock divided by 2.

0: - DAC system clock is DAXCK (default)

1: - DAC system clock is DAXCK/2

MUTE56: Mute control for channels 5 and 6

0: do not mute channels 5 and 6

1: simultaneously mute channels 5 and 6

MUTE34: Mute control for channels 3 and 4

0: do not mute channels 3 and 4

1: simultaneously mute channels 3 and 4

MUTE12: Mute control for channels 1 and 2

0: do not mute channels 1 and 2

1: simultaneously mute channels1 and2

---

**CREG2 - 7, DAC Volume Registers for channel 1 to 6, (ADRS=hex02 - hex07, default=hex80)**

ADDR[3:0]	Volume Registers							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 02	Channel 1 left volume register, VOLREGL1[7:0]							
Hex 03	Channel 1 right volume register, VOLREGR1[7:0]							
Hex 04	Channel 2 left volume register, VOLREGL2[7:0]							
Hex 05	Channel 2 right volume register, VOLREGR2[7:0]							
Hex 06	Channel 3 left volume register, VOLREGL3[7:0]							
Hex 07	Channel 3 right volume register, VOLREGR3[7:0]							
Default Value	1	0	0	0	0	0	0	0

VOLREG:- Control the volume of the 6 DAC's

80h corresponds to 0 dB and 02h to -64 dB. in -0.5 db step. Value should not be programmed greater than 80h.

**CREG 8, ADC Proc Register (ADRS=hex08, default=hex82)**

ADDR[3:0]	CREG0[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 08	NGATE	NGTH[1:0]		ALCHTM	ALCEN	ALC[2:0]		
Default Value	1	0	0	0	0	0	1	0

NGATE: Noise Gate

0: - Noise Gate Disabled.

1: -Noise Gate Enable. When the signal level is lower than the level specified by the NGTH the ADC output will be zeroed.

NGTH[1:0]: - Specified the Noise Gate Threshold.

00: - -66dB

01: - -72 dB.

10: - -78dB.

11: - -84 dB.

ALCHTM: - Automatic Level Control Hold time.

0: - 340 ms. (default). For music program.

1: - 5.3 ms. This should be used for speech conversion.

ALCEN: - Enable Automatic Level Control Function

0: - Disable ALC. (default)

1: - Enable ALC.

ALC[2:0]: - ALC Target Level.

000: - -1 dB.

001: - -2 dB.

010: - -3 dB. (default)

011: - -4 dB.

100: - -5 dB.

101: - -6 dB.

110: - -7 dB.

111: - -8 dB.

**CREG9, ADC Control Register (ADRS=hex09, default=hexA0)**

ADDR[3:0]	CREG0[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 09	FMT[1:0]		NBIT[1:0]		X	SRC[1:0]		CKDIV2
Default Value	1	0	1	0	0	0	0	0

MT[1:0] Digital Serial Bus Format Select for ADC.

00: - Normal or Right Justified Format.

01: -Left Justified Format.

10: - I2S Format.(default)

11: - TDM, Multi-channel Time Division Multiplex Format

NBIT[1:0]: - These two bits define the ADC serial audio input resolution for right justified and TDM mode

00: - 16-bit resolution.

01: - 20-bit resolution.

10: - 24-bit resolution (default).

11: - 32-bit resolution.

SRC[1:0]: - ADC Sampling Rate Selection. It is used in the ADC Master Mode, CRA[1]=1, to generate ADFS and ADBCK.

00: - Sampling Rate = XCK/256.

01: - Sampling Rate = XCK/128.

10: - Sampling Rate = XCK/384.

11: - Sampling Rate = XCK/192.

CKDIV2: - Enable the ADXCK Clock divided by 2.

0: - ADC system clock is ADXCK (default)

1: - ADC system clock is ADXCK/2



**CREGA, Chip Control Register (ADRS=hex0A, default=hex00)**

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 0A	DAMSTR	DAPWD	X	X	ADMSTR	ADPWD	ZCBYP	HPFBYP
Default Value	0	0	0	0	0	0	0	0

DAMSTR: Configure the DAC PCM Serial Port.

- 0: - Slave Mode
- 1: - Master Mode.

DAPWD: DAC Power Down

- 0: DAC enabled
- 1: DAC Power Down.

ADMSTR: Configure the ADC PCM Serial Port.

- 0: - Slave Mode
- 1: - Master Mode.

ADPWD: ADC Power Down

- 0: ADC enabled
- 1: ADC Power Down.

ZCBYP: Disable ADC Zero Crossing Detection

- 0: Zero crossing is enabled.
- 1: Zero crossing is bypassed.

HPFBYP: Bypass ADC data path High Pass Filter

- 0: Enable high pass filter.
- 1: Disable high pass filter.

**CREGB, ADC Input Enable (ADRS=hex0B, default=hex01)**

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 0B	X	X	X	AMUX[4:0]				
Default Value	1	0	0	0	0	0	0	1

AMUX[4:0]: ADC Input Channel Enable.

00001: - AIN1

00010: - AIN2

00100: - AIN3

01000: - AIN4

10000: - AIN5

**CREGC, ADC Input Gain Selection (ADRS=hex0C, default=hex99)**

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 0C	LGAIN[3:0]				RGAIN[3:0]			
Default Value	1	0	0	1	1	0	0	1

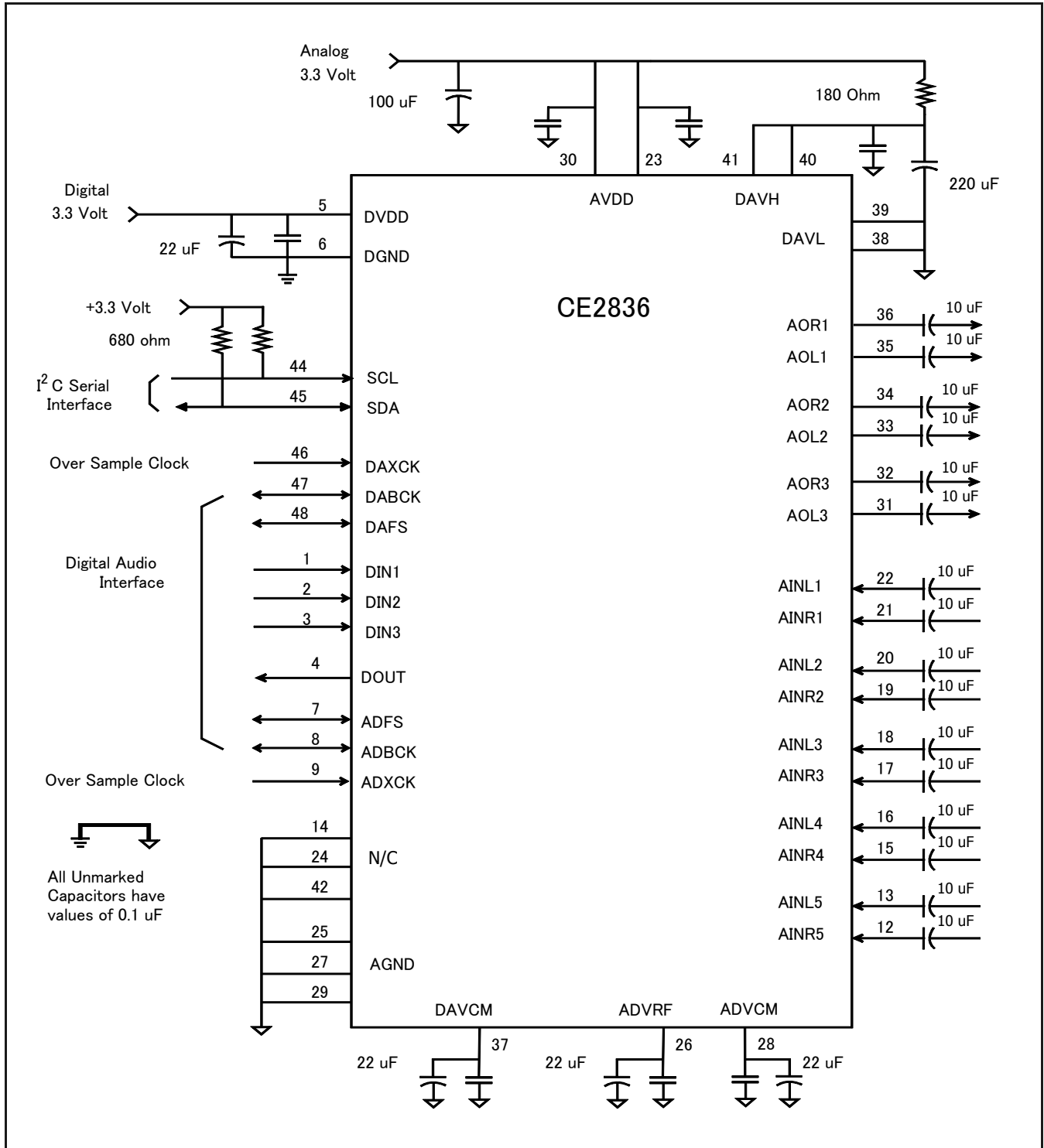
LGAIN[3:0] is for ADC Left Channel Gain Select While RGAIN[3:0] is for Right Channel Gain Select  
1111 corresponds to +6 dB and 0000 to -9 dB with -1dB step

**CREGD, Chip Soft Reset (ADRS=hex0D, default=hex92)**

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 0D	RESET[7:0]							
Default Value	1	0	0	1	0	0	1	0

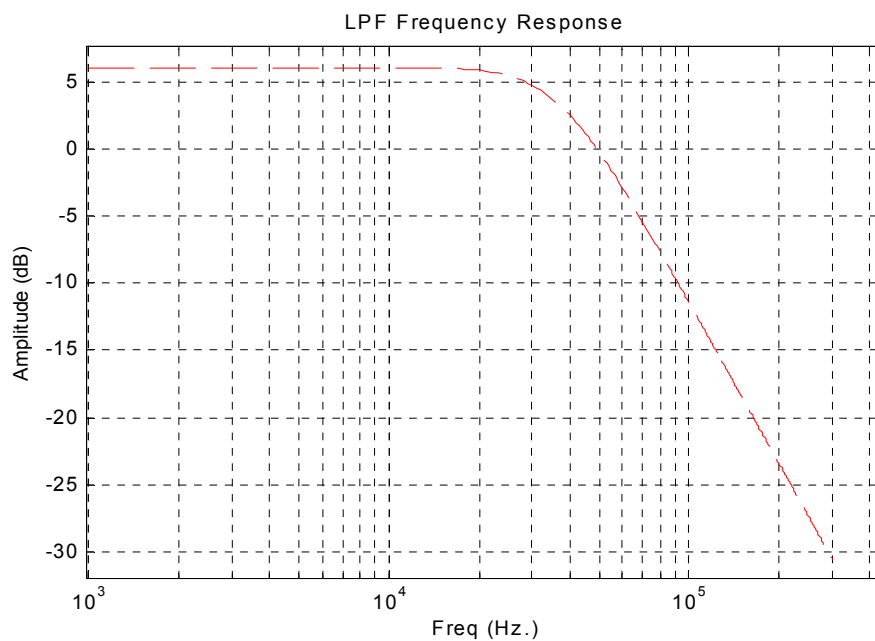
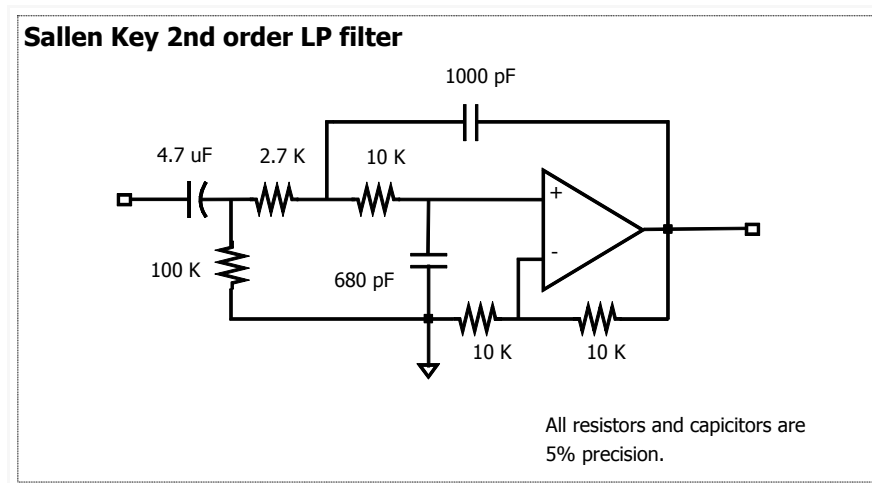
Chip Soft Reset; A write of all zeros to this register will reset the chip except the Command Registers.  
Another write of hex92 is required to enable to chip again.

APPLICATION CONNECTION EXAMPLE:



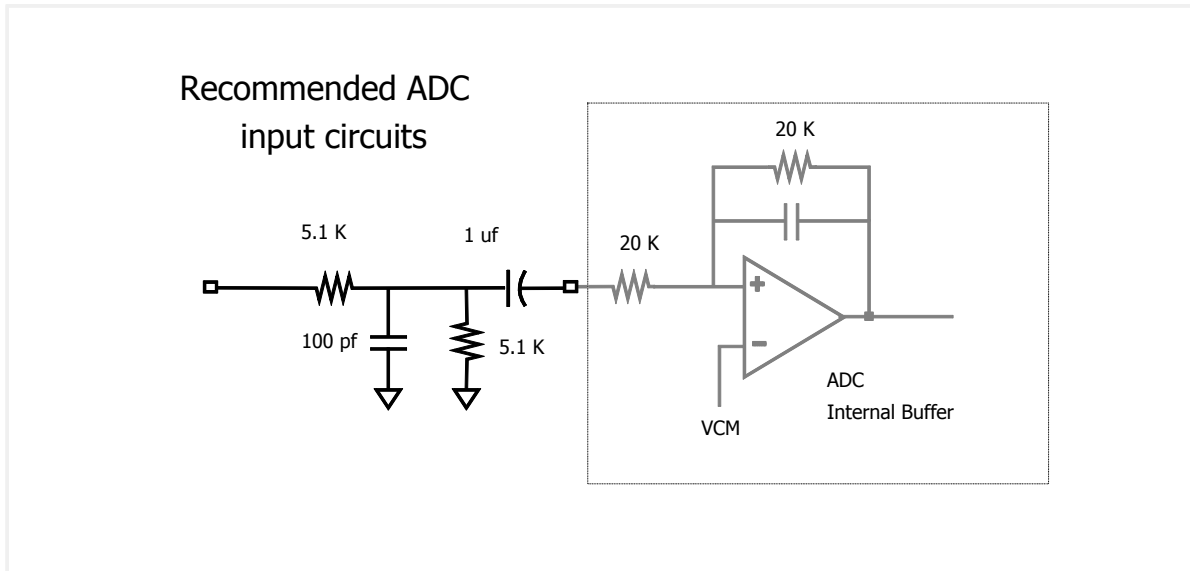
## SUGGESTED ANALOG RECONSTRUCTION FILTER

A second Sallen Key low pass reconstruction filter is recommended to remove the high frequency sigma delta modulator noise. The filter's component values and characteristic are shown in the following figures.



## ADC

The ADC converters have a input buffer. The buffers have a equivalent input resistance of 20K ohm. To ensure the performance it is recommended that the applications should have a simple low pass filter to remove the high frequency noise.



TIMING DIAGRAM

Figure 3. Audio Serial Interface Timing Requirement

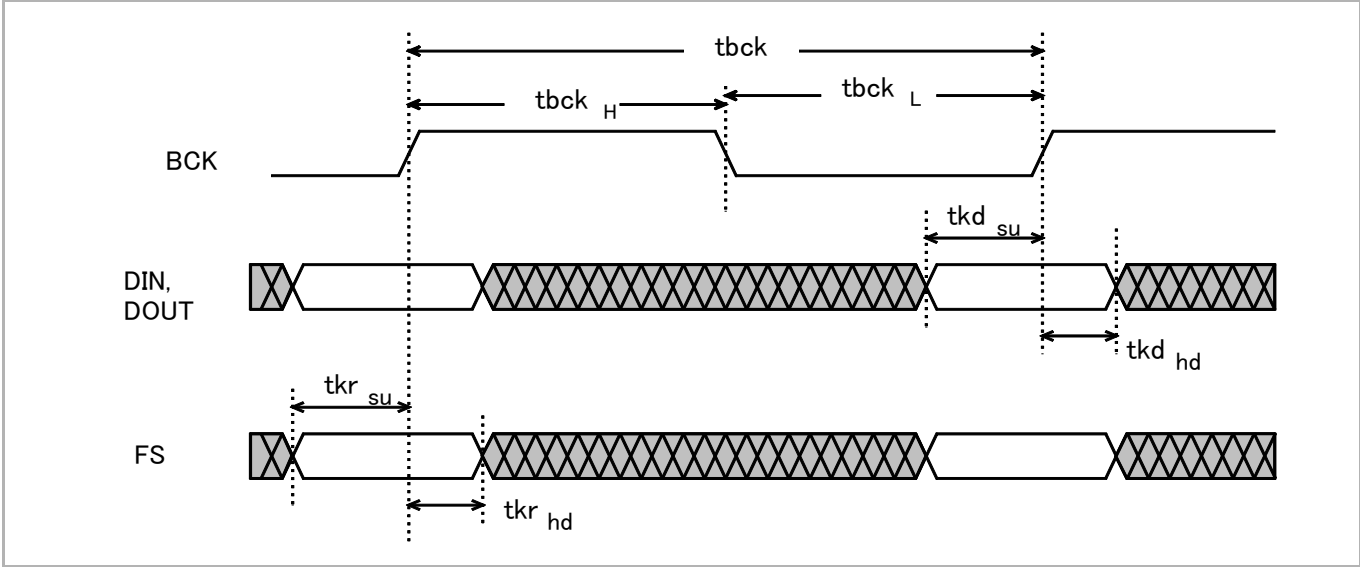
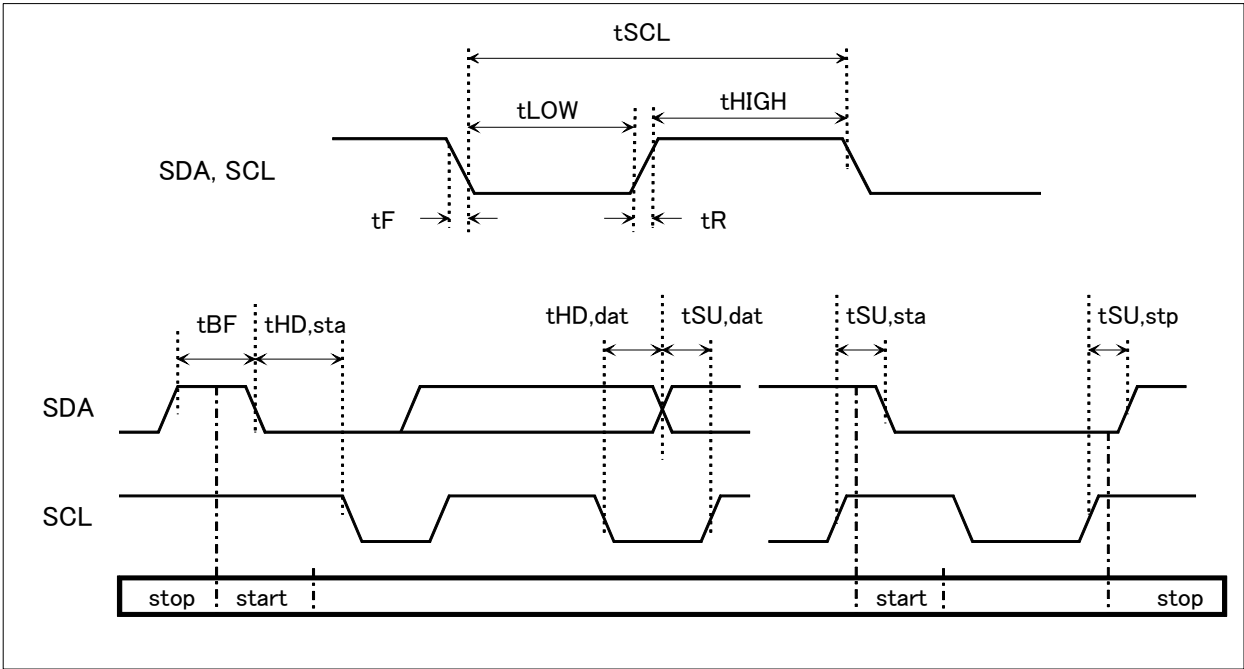


Figure 4. Serial Command Port Write Timing Requirement



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**ABSOLUTE MAXIMUM RATINGS**

Symbol	Characteristics	Min	Max	Units
V <sub>DD</sub>	Power Supply Voltage (Measured to GND)	-0.5	+7.0	V
V <sub>i</sub>	Digital Input Applied Voltage <sup>2</sup>	GND-0.5		V
A <sub>i</sub>	Digital Input Forced Current <sup>3,4</sup>	-100	100	mA
V <sub>o</sub>	Digital Output Applied Voltage <sup>2</sup>	GND-0.5	V <sub>DD</sub> +0.5	V
A <sub>o</sub>	Digital Output Forced Current <sup>3,4</sup>	-100	100	mA
TDsc	Digital Short Circuit Duration (single output high state to Vss)		1	Sec
TA <sub>SC</sub>	Analog Short Circuit Duration (single output to VSS1)		infinite	Sec
T <sub>a</sub>	Ambient Operating Temperature Range	-25	+125	°C
T <sub>j</sub>	Junction Temperature (Plastic Package)	-65	+150	°C
Tsol	Lead Soldering Temperature (10 sec., 1/4" from pin)		280	°C
Tvsol	Vapor Phase Soldering (1 minute)		220	°C
Tstor	Storage Temperature	-65	+150	°C

## Notes:

1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.
2. Applied voltage must be current limited to specified range, and measured with respect to VSS.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

**ELECTRICAL CHARACTERISTICS**

Parameter	Characteristics	Min	Typ	Max	Units
<b>Power Supply</b>					
AVDD	Analog power supply voltage	2.8	3.3	4.0	V
DVDD	Digital power supply voltage	2.8	3.3	4.0	V
I <sub>DA</sub>	Analog Current		60		mA
I <sub>DD</sub>	Digital Current		20	18	mA

**Audio DAC Characteristics**

	Full Scale Output Voltage to a 10K load	.98	1	1.02	V <sub>rms</sub>
V <sub>VCM</sub>	Reference voltage		VDD/2		V

**Digital Characteristics**

V <sub>IH</sub>	Digital Input Voltage, Logic HIGH, TTL Compatible Inputs.	2.0		V <sub>DD</sub>	V
I <sub>OZH</sub>	Hi-Z Leakage Current, HIGH, V <sub>DD</sub> =Max, V <sub>IN</sub> =3.3 Volt			33	μ A
I <sub>OZL</sub>	Hi-Z Leakage Current, LOW, V <sub>DD</sub> =Max, V <sub>IN</sub> =V <sub>SS</sub> )			-10	μ A
C <sub>I</sub>	Digital Input Capacitance (T <sup>A</sup> =25°C, f=1Mhz)			8	pF
C <sub>O</sub>	Digital Output Capacitance (T <sup>A</sup> =25°C, f=1Mhz)			10	pF

**Audio Serial Interface Timing**

tbck	BCK Cycle Time	80			ns
tbck <sub>H</sub>	BCK Pulse Width, HIGH	30			ns
tbck <sub>L</sub>	BCK Pulse Width, LOW	30			ns
tkd <sub>su</sub>	Audio Data Setup Time With Respect To Rising Edge of BCK	10			ns
tkd <sub>hd</sub>	Audio Data Hold Time With Respect to Rising Edge of BCK	15			ns
tkr <sub>su</sub>	Audio FS Setup Time With Respect To Rising Edge of BCK	10			ns



Parameter	Characteristics	Min	Typ	Max	Units
t <sub>kr<sub>hd</sub></sub>	Audio FS Hold Time With Respect To Rising Edge of BCK	15			ns

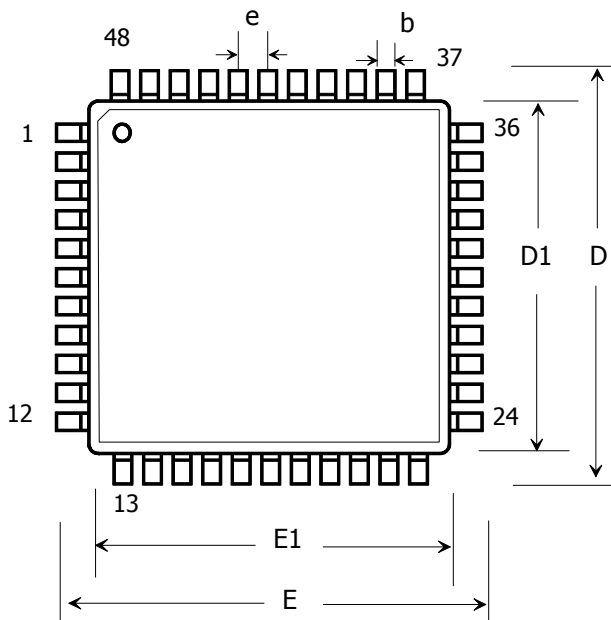
#### Serial Command Port

fSCL	SCL Clock Frequency			100	kHz
t <sub>SU,sta</sub>	Start condition set up time	4.7			us
t <sub>HD,sta</sub>	Start condition hold time	4.0			us
t <sub>SU,stp</sub>	Stop condition set up time	4.0			us
t <sub>LOW</sub>	SCL Low time	4.7			us
t <sub>HIGH</sub>	SCL High time	4.0			us
t <sub>R</sub>	SCL & SDA rise time			1.0	us
t <sub>F</sub>	SCL & SDA fall time			0.3	us
t <sub>SU,DAT</sub>	Data set-up time	250			ns
t <sub>HD,DAT</sub>	Data hold time	0			ns
t <sub>BF</sub>	Bus Free time	4.7			us

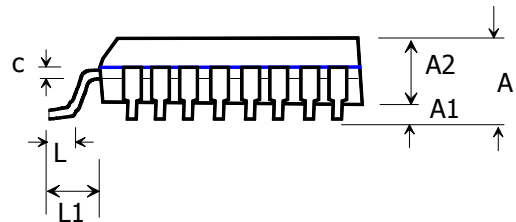
PACKAGING INFORMATION (LQFP 48 PIN)

Dimensions

SYMBOLS	mm.			SYMBOLS	mm.		
	min	norm	max		min	norm	max
A			1.68	E	9.0 BSC		
A1	0.05		0.15	E1	7.0 BSC		
A2	1.35	1.4	1.45	e	0.45	0.65	0.75
b	0.17	0.22	0.27	L	0.63	0.6	1.03
C	0.09		0.20	L1	1.00 REF		
D	9.0 BSC						
D1	7.0 BSC						



LQFP 48 (7 X 7 mm)



# Digital Power Amplifier R2S15102NP

## 10Wx2ch(SE)/20Wx1ch(BTL) Digital Audio Power Amplifier

### 1. Outline

R2S15102NP is a Digital Power Amplifier IC developed for TV.

R2S15102NP can realize maximum Power 10W x 2ch

(VD = 24V, THD = 10%, SE) at 8 Ω load.

It is possible to replace from the conventional analog amplifier system to the digital amplifier system easily.

### 2. Feature

- High Output Power (THD=10%) without external Heat Sink  
(note) the thermal pad is soldered the thermal pad with the printed-circuit board directly.

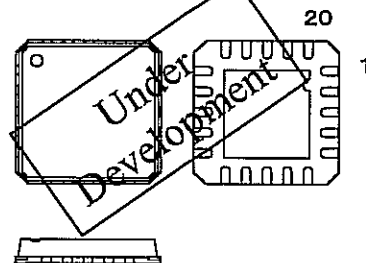
Recommended Power Condition

SE operation mode : 10Wx2ch (VD=24V) at 8 Ω

BTL operation mode: 20Wx1ch (VD=18V) at 8 Ω

- The RENESAS original circuits realize high power efficiency, low noise and low distortion characteristics.
- Pop sound Less
- Built-in protection function  
(Over Current, Over Temperature and Under Voltage)
- Built-in Mute and Stand-by function

Fig. 1 Package

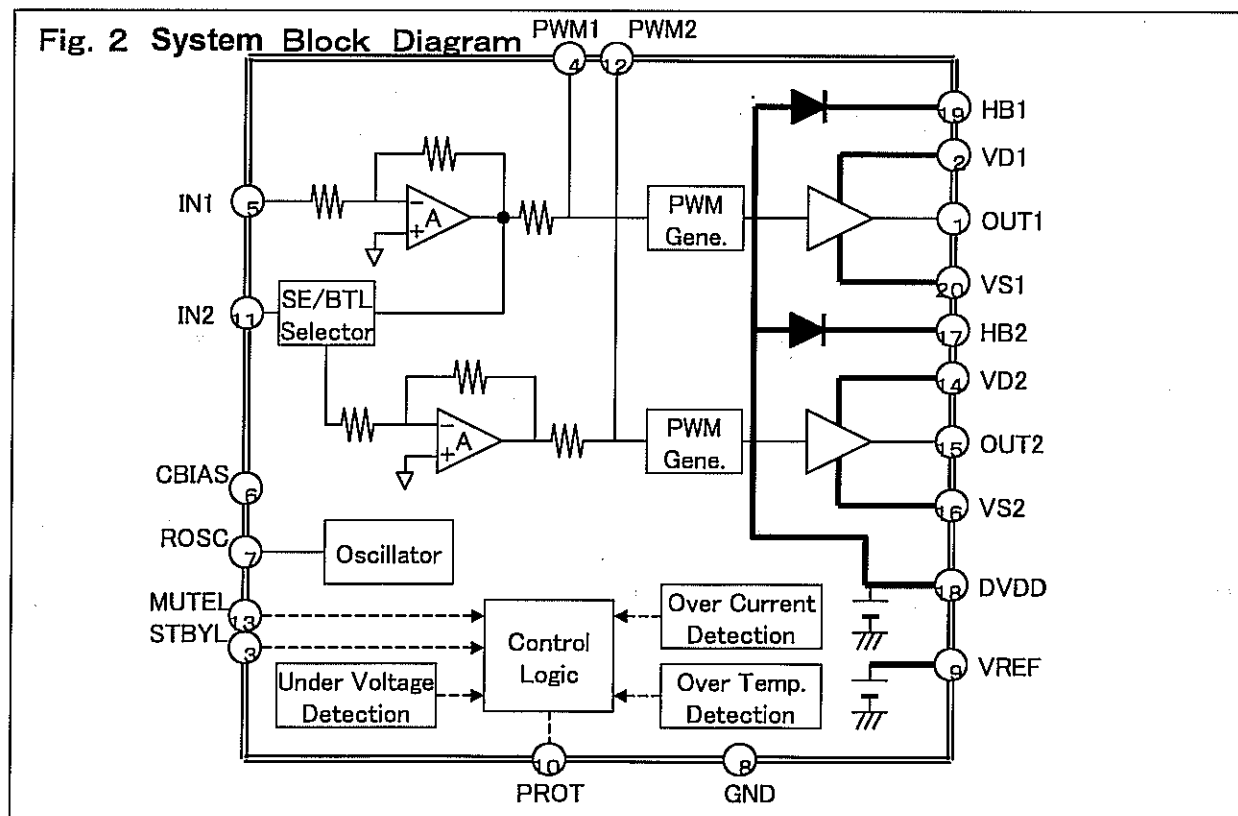


20pin QFN  
Body : 6 x 6 mm  
Lead pitch : 0.8 mm

### 3. Operating Condition

- Recommended Power supply voltage : from 11V to 25V
- Recommended Speaker Impedance : from 4 to 8Ω

### 4. Block Diagram



## Digital Power Amplifier R2S15102NP

### 5. Pin Configuration(Table.1)

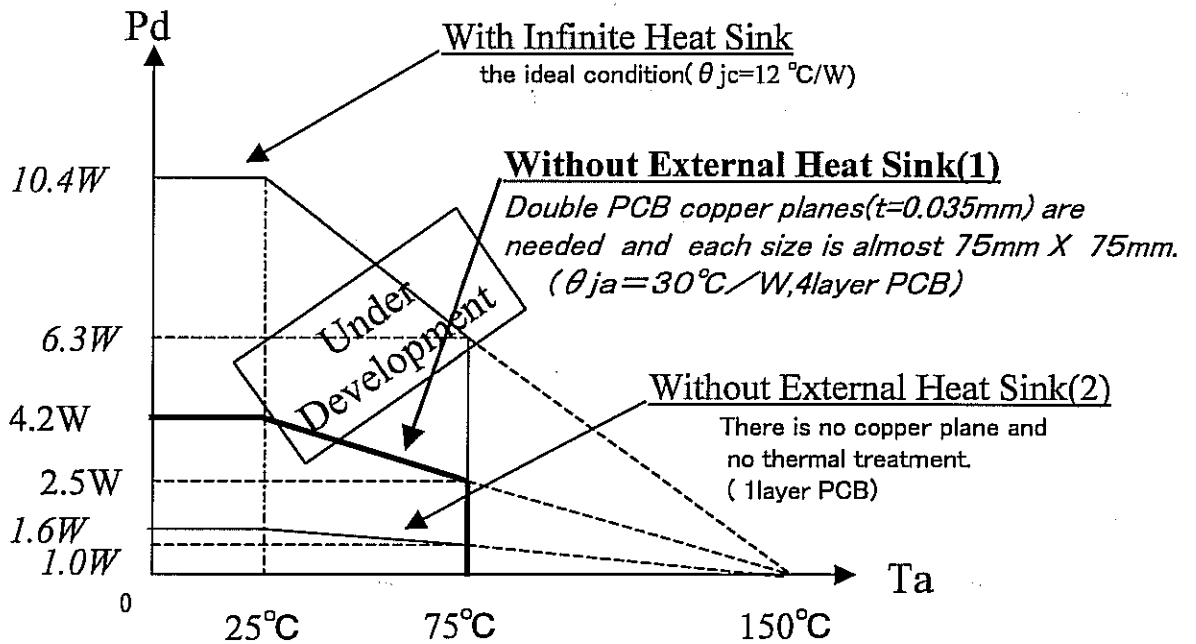
No.	NAME	I/O	Description	
1	OUT1	O	Power Output pin #1	
2	VD1	—	Power supply pin for power output stage #2	
3	STBYL	I	Stand-by control pin. When this is “L”, circuit current is reduced. There is the pull-down resistor:50Kohm(typ.).	
4	PWM1	I	PWM input pin #1 ( for phase compensation)	
5	IN1	I	Analog input #1. The gain is depended on the external resistance .	
6	CBIAS	I/O	A capacitor is connected so that it may not be influenced of power supply change(Ripple Filter).	
7	ROSC	I	Control pin for PWM carrier frequency	
8	GND	—	GND pin for analog block	
9	VREF	I/O	Capacitor connection pin for analog block reference voltage source	
10	PROT	O	Protection Timer pin. At protection mode,the output becomes “L”-level. (The timing capacitor is connected)	
11	IN2	I	SE operation	Analog input #2(as same as IN1)
		I	BTL operation	When this is connected to DVDD pin via the resistor, Reversed signal of OUT1 is output to OUT2.
12	PWM2	I	PWM input pin#2 ( for phase compensation)	
13	MUTEL	I	Mute control pin. When this is “L”, it becomes mute status.	
14	VD2	—	Power supply pin for power output stage #2	
15	OUT2	O	Power Output pin #2	
16	VS2	—	Ground pin for power output stage #2	
17	HB2	I/O	Capacitor connection pin for bootstrap	
18	DVDD	O	Built-in power supply pin for internal digital block.	
19	HB1	I/O	Capacitor connection pin for bootstrap #1	
20	VS1	—	Ground pin for power output stage #1	

# Digital Power Amplifier R2S15102NP

## 6. Absolute Maximum Rating (Table.2)

Symbol	Parameter	Condition	Value	Unit
VD max	Maximum VD Voltage	VD1, VD2 pin voltage	27	V
HB max	Maximum HB Voltage	HB1, HB2 pin voltage	40	V
Pd	Power dissipation	Ta = 25°C : See Fig.3	4.2	W
$\theta_{ja}$	Thermal Resistance	See Fig.3	30	°C/W
Tj	Junction temperature	Maximum Temperature	150	°C
Ta	Operating ambient temperature	Temperature range	-20~75	°C
Tstg	Storage temperature	Temperature range	-40~150	°C

**Fig.3 Thermal De-rating (on PCB: printed-circuit board ): Size 75mm x 75mm**

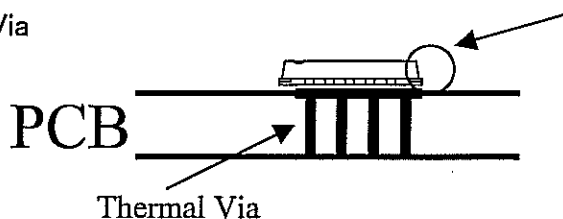


**(NOTE)**

**PCB pattern design for high effective thermal conductivity**

(1) The exposed die pad is directly soldered with the printed-circuit board pattern.

(2) Thermal Via



(caution)  
There are side exposures of the die pad at corners of the package.  
(The die pad is grounded.)

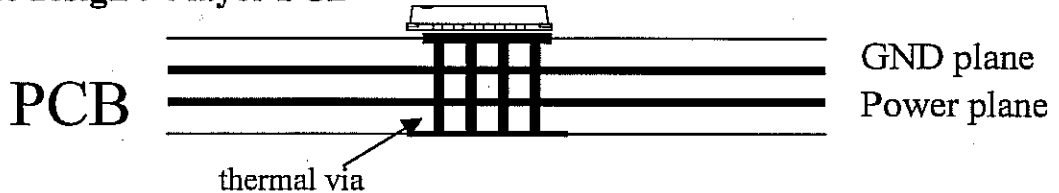
# Digital Power Amplifier R2S15102NP

## Consideration about the PCB design

The Power dissipation at 10Wx2ch(SE) or 20Wx1ch(BTL) is estimated almost 2W. It has enough margin, designing the PCB at  $\theta_{ja}=30^{\circ}\text{C}/\text{W}$ .

### (1)PCB basic design (copper plane)

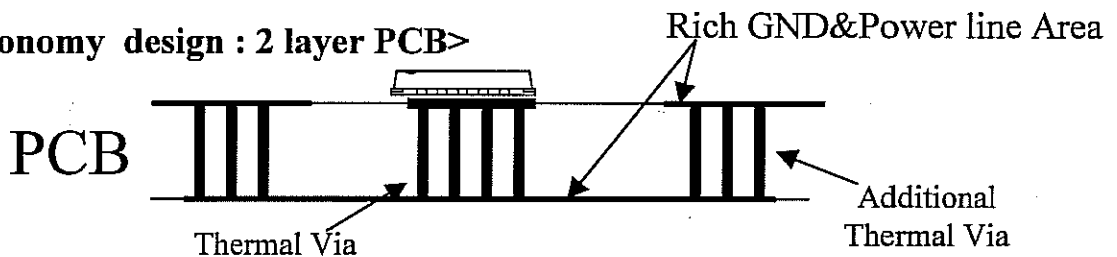
<the best design : 4 layer PCB>



<PCB size estimation >

10Wx2ch: 75mm x 75mm

<the economy design : 2 layer PCB>



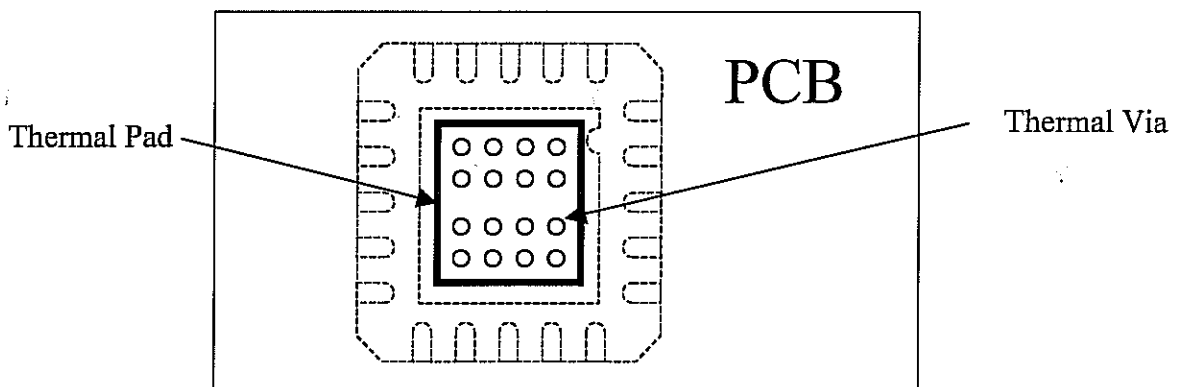
The GND&Power line total area size is also equal to the above GND&Power line total area size of the 4layer PCB.

<PCB size estimation >

10Wx2ch:  $(75 + \alpha)$  mm x  $(75 + \alpha)$  mm

### (2)PCB Thermal Pad

The exposed die pad is directly soldered with the printed-circuit board pattern .



# Digital Power Amplifier R2S15102NP

## 7. Recommended Operating condition(Table.3)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VD	Supply Voltage	VD1,VD2 pin voltage	11	-	25	V
VH	Control voltage of high level	STBYL, MUTEL	2	-	5	V
VL	Control voltage of low level	STBYL, MUTEL	0	-	0.8	V
fosc	Carrier Frequency	R= 33kΩ	300	400	600	kHz

- (note)
- STBYL: High level:normal operation      Low level:Stand-by
  - MUTEL:High level:normal operation      Low level:Mute
  - The carrier frequency can be changed by the resistance at Pin#.7 .

## 8. Electronic Characteristics(Table.4)

(Unless otherwise noted, Ta=25°C, VD=24V, Carrier Frequency=400kHz, f=1kHz, SE operation)

Symbol	Parameter		Condition	MIN	TYP	MAX	Unit
IVD	Circuit Current		No Signal	TBD	28	TBD	mA
			MUTE	TBD	-	TBD	mA
			Stand-by	-	-	10	uA
VDPR	Detection Voltage		VD under-voltage	TBD	9.8	TBD	V
TPR	Protection Temperature		Thermal Shut-dawn	-	150	-	°C
TRL	Release Temperature		Thermal Shut-dawn	-	120	-	°C
IPR	Protection Current		Output over-current	-	6	-	A
Pomax	Maximum output power	at SE	THD=10%、VD=24V、RL=8Ω	TBD	10	-	W/ch
		at BTL	THD=10%、VD=18V、RL=8Ω	TBD	20	-	W
THD	Total Harmonic Distortion		Po=1W	-	0.1	TBD	%
No	Output Noise level		A-Weighted filter	-	(100)	TBD	uVrms
Eff	Power Efficiency	at SE	Po=10+10W	TBD	93	-	%
		at BTL	Po=20W	TBD	89	-	%
Mute	Mute Attenuation			TBD	80	-	dB
PSRR	Ripple Rejection Ratio		dVD=100mVrms,f=100Hz	TBD	50	-	dB

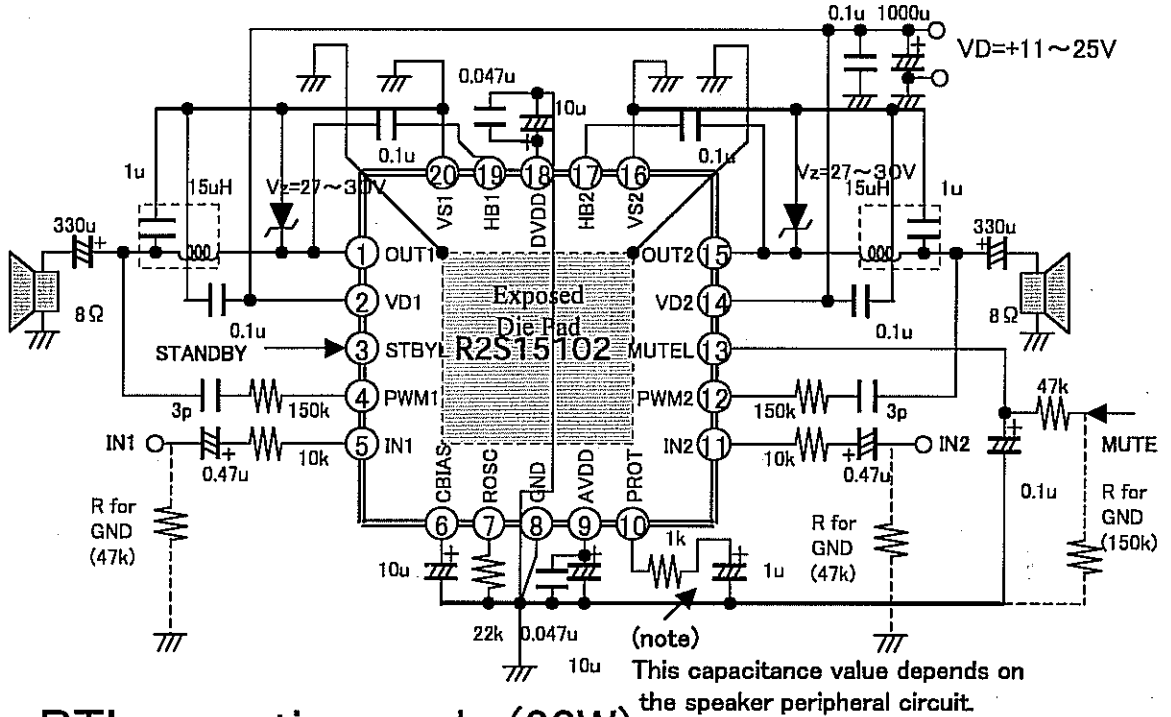
# Digital Power Amplifier R2S15102NP

## 9. Application Examples

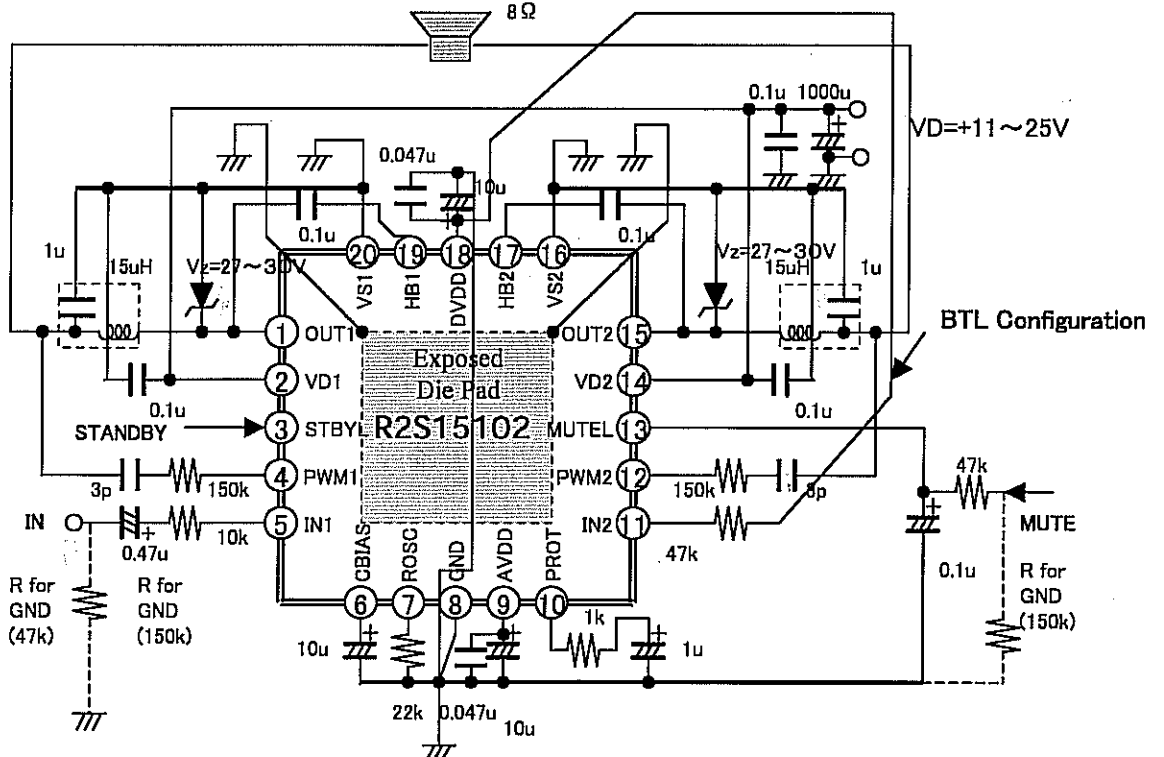
### Fig.4 SE operation mode(10Wx2ch)

(note)

“R for GND” ‘s are for the evaluation only and not needed actually.



### Fig.5 BTL operation mode (20W)

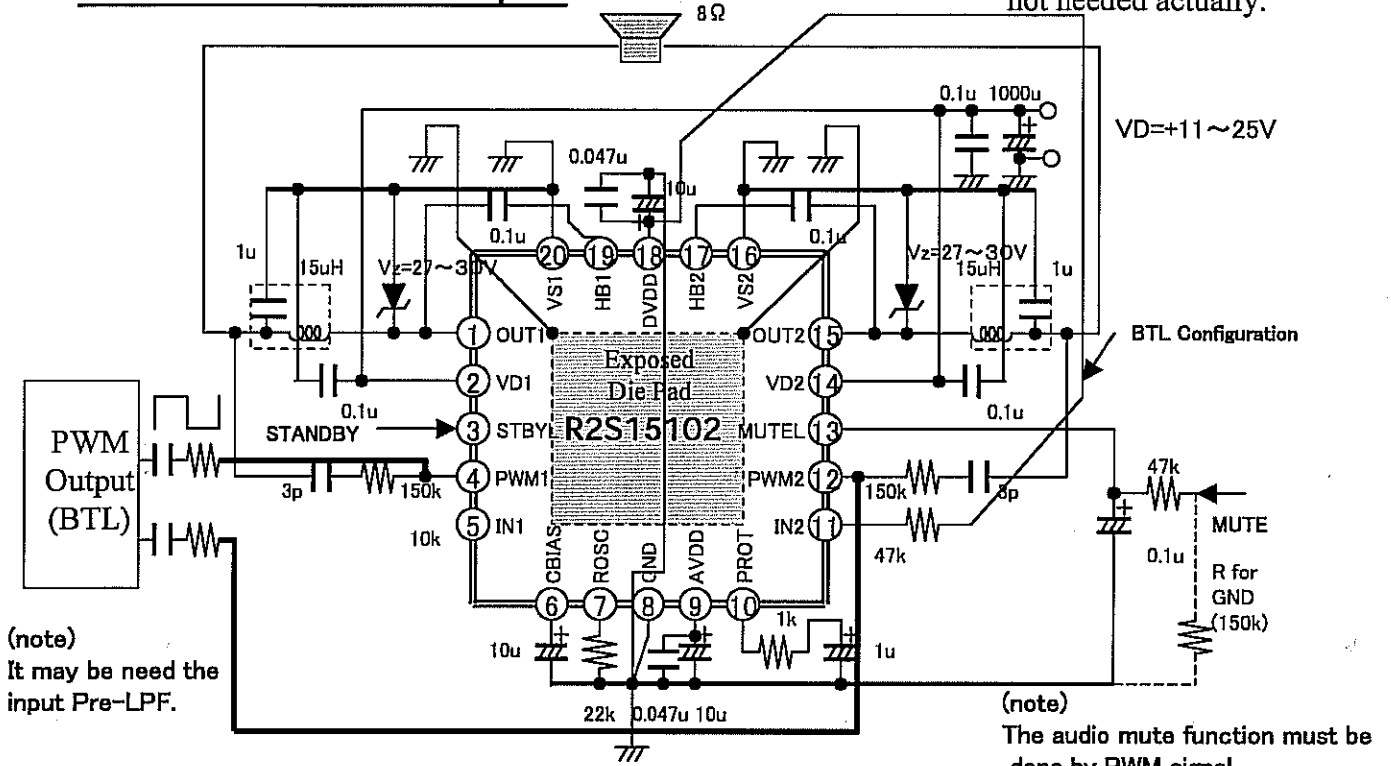




# Digital Power Amplifier R2S15102NP

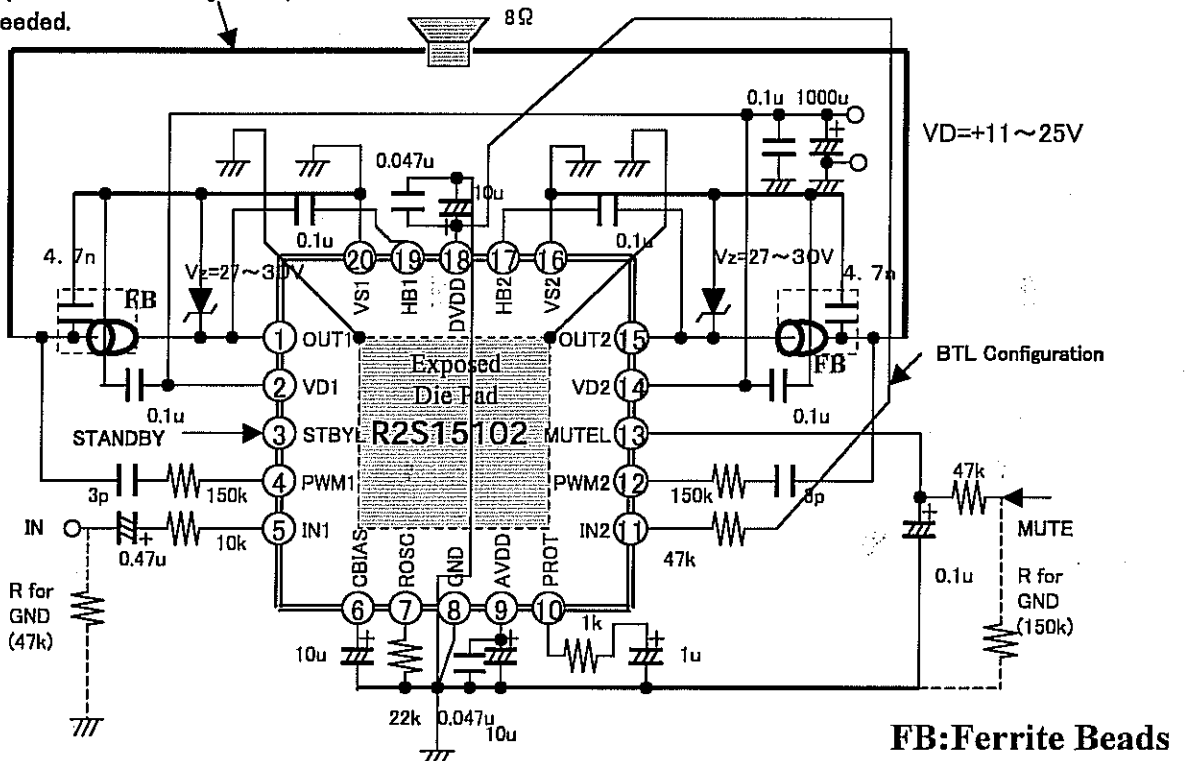
**Fig.6 BTL operation mode(20W)  
with PWM direct input**

(note)  
"R for GND" 's are  
for the evaluation only and  
not needed actually.



**Fig.7 BTL operation mode without output LPF coil**

If this speaker lines is very short,  
the LPF coil  
is not needed.



Product Specification

# SPECIFICATION FOR APPROVAL

- ( ) Preliminary Specification
- (●) Final Specification

Title	42.0" WXGA TFT LCD
-------	--------------------

BUYER	
MODEL	

SUPPLIER	LG.Philips LCD Co., Ltd.
*MODEL	LC420W02
SUFFIX	SLA1 (Lead Free)

\*When you obtain standard approval, please use the above model name without suffix

APPROVED BY	SIGNATURE DATE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE DATE
J.J Kim / S. Manager	06-3-03
REVIEWED BY	
K. S Choi / Manager	06-3-03
PREPARED BY	
S. W Kwag / Engineer	06-3-03

TV Products Development Dept.  
LG. Philips LCD Co., Ltd

Version: 1.0 Date: 2006.03.03

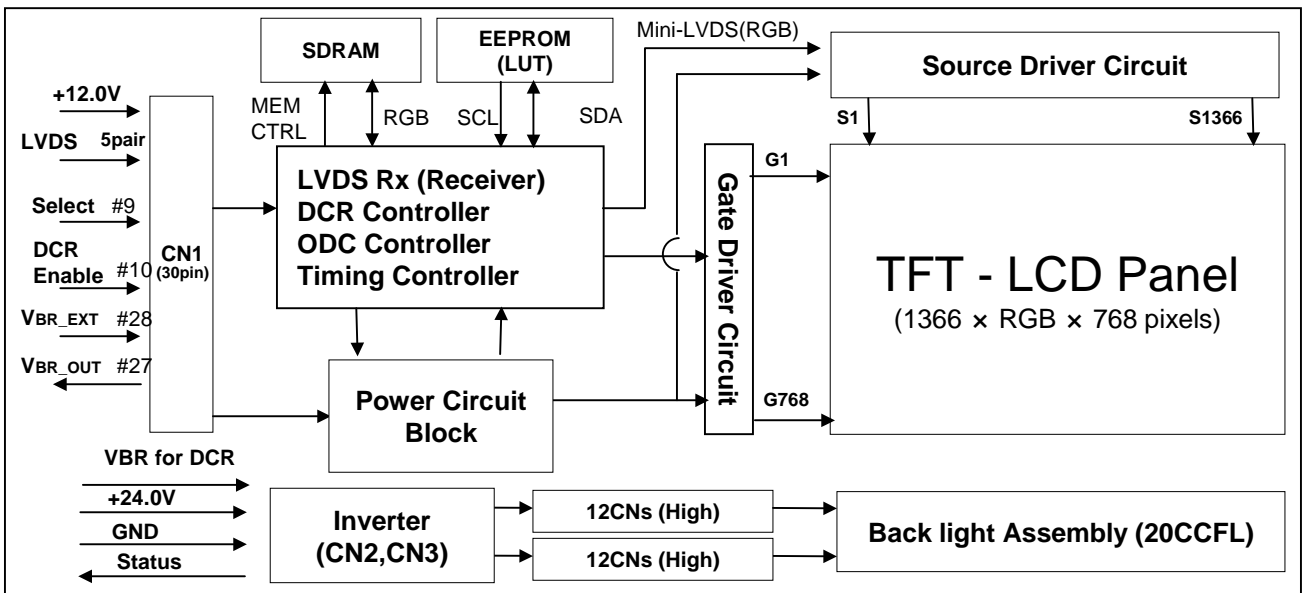
Product Specification

## 1. General Description

The LC420W02 is a Color Active Matrix Liquid Crystal Display with an integral Cold Cathode Fluorescent Lamp(CCFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 42.0 inch diagonally measured active display area with WXGA resolution (768 vertical by 1366 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot, thus presenting a palette of more than 16.7M(true) colors.

It has been designed to apply the 8-bit 1-port LVDS interface.

It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



## General Features

Active Screen Size	42.02 inches(1067.308mm) diagonal
Outline Dimension	1006 mm(H) x 610 mm(V) x 56 mm(D) (Typ.)
Pixel Pitch	0.227mm x 0.681mm x RGB
Pixel Format	1366 horiz. by 768 vert. Pixels RGB stripe arrangement
Color Depth	8-bit, 16.7 M colors
Luminance, White	500 cd/m <sup>2</sup> (Center 1-point) (Typ.)
Viewing Angle (CR>10)	Viewing Angle Free ( R/L 178 (Typ.), U/D 178 (Typ))
Power Consumption	Total 167.7W (Typ.) (Logic=5.7W, Inverter=162W [I <sub>BL</sub> =6.5mA] )
Weight	14.5Kg (Typ.)
Display Operating Mode	Transmissive mode, Normally black
Surface Treatment	Hard coating(3H), Anti-glare treatment of the front polarizer

Product Specification

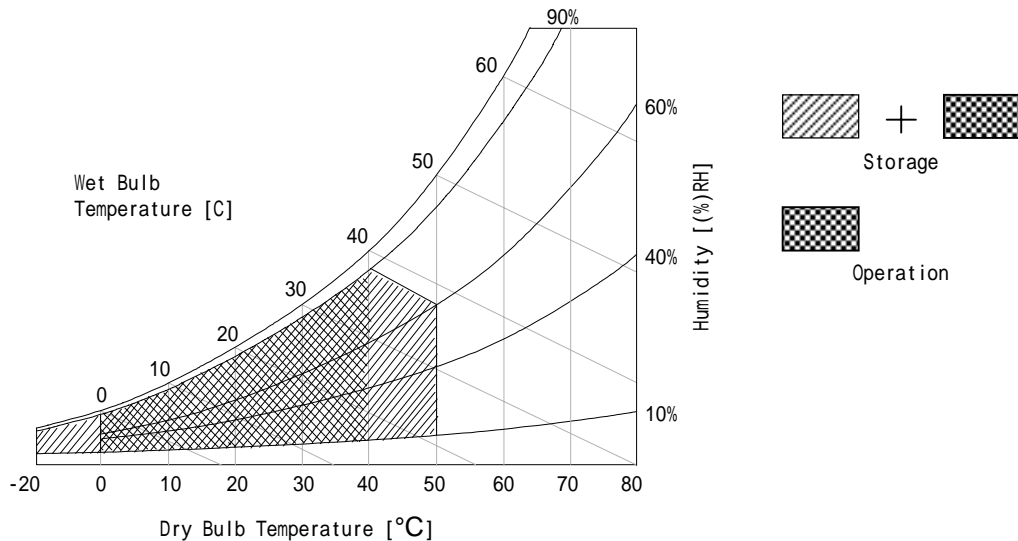
## 2. Absolute Maximum Ratings

The following items are maximum values which, if exceeded, may cause faulty operation or damage to the LCD module.

**Table 1. ABSOLUTE MAXIMUM RATINGS**

Parameter		Symbol	Value		Unit	Remark
			Min	Max		
Power Input Voltage	LCD circuit	V <sub>LCD</sub>	-0.3	+14.0	V <sub>DC</sub>	at 25 ± 2 °C
	Inverter	V <sub>BL</sub>	21.6	+27.0	V <sub>DC</sub>	
Inverter Control Voltage	ON/OFF	V <sub>OFF/VON</sub>	-0.30	+5.25	V <sub>DC</sub>	
	Brightness	V <sub>BR</sub>	0.0	+5.0	V <sub>DC</sub>	
Operating Temperature		T <sub>OP</sub>	0	+40	°C	Note 1
Storage Temperature		T <sub>ST</sub>	-20	+50	°C	
Operating Ambient Humidity		H <sub>OP</sub>	10	90	%RH	
Storage Humidity		H <sub>ST</sub>	10	90	%RH	

Note 1. Temperature and relative humidity range are shown in the figure below.  
Wet bulb temperature should be 39 °C Max, and no condensation of water.



Product Specification

### 3. Electrical Specifications

#### 3-1. Electrical Characteristics

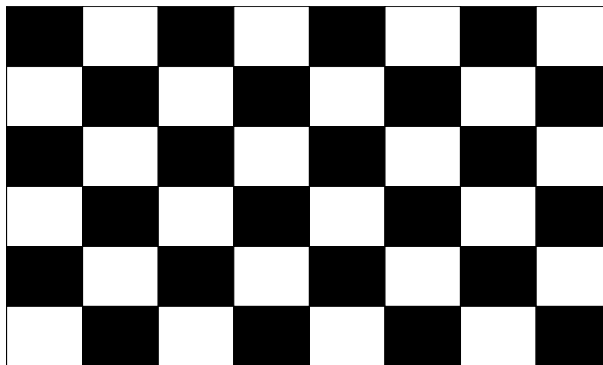
It requires two power inputs. One is employed to power for the LCD circuit. The other input power for the CCFL/Backlight is to power inverter.

**Table 2. ELECTRICAL CHARACTERISTICS**

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Circuit :						
Power Input Voltage	VLCD	11.4	12.0	12.6	VDC	
Power Input Current	ILCD	-	475	618	mA	1
		-	680	884	mA	2
Power Consumption	PLCD		5.7	7.42	Watt	1
Rush current	IRUSH	-	-	3.0	A	3

- Note :
1. The specified current and power consumption are under the  $V_{LCD}=12.0V$ ,  $25 \pm 2^{\circ}C$ ,  $f_V=60Hz$  condition whereas mosaic pattern(8 x 6) is displayed and  $f_V$  is the frame frequency.
  2. The current is specified at the maximum current pattern.
  3. The duration of rush current is about 2ms and rising time of power input is 1ms (min.).

White : 255Gray  
Black : 0Gray



Mosaic Pattern(8 x 6)

Product Specification

**Table 3. ELECTRICAL CHARACTERISTICS (Continue)**

Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
Inverter :							
Power Supply Input Voltage		VBL	22.8	24.0	25.2	Vdc	1
Power Supply Input Voltage Ripple			-0.2		0.2	Vp-p	
Power Supply Input Current		IBL	-	6.75	7.2	A	
Power Consumption		PBL	-	162	172.8	W	
Input Voltage for Control System Signals	Brightness Adjust	VBR	0.0	-	3.3	Vdc	2
	On/Off	On	V on	4.0	-	5.0	Vdc
		Off	V off	-0.3	0.0	0.5	Vdc
Lamp :							
Life Time			50,000			Hrs	3

Notes :

- Electrical characteristics are determined after the unit has been 'ON' and stable for approximately 120 minutes at  $25 \pm 2^\circ\text{C}$   
The specified current and power consumption are under the typical supply Input voltage 24V and Vbr 3.3V, it is total power consumption.  
The ripple voltage of the power supply input voltage is under 0.2 Vp-p.  
LPL recommend Input Voltage is  $24.0\text{V} \pm 5\%$ .
- Brightness Control.  
This VBR Voltage control brightness.

VBR Voltage	Function
3.3V	Maximum Brightness (100%)
0V	Minimum Brightness.(25%)

- The life is determined as the time at which luminance of the lamp is 50% compared to that of initial value at the typical lamp current on condition of continuous operating at  $25 \pm 2^\circ\text{C}$ .  
Specified value is when lamp is aligned horizontally.

Product Specification

### 3-2. Interface Connections

This LCD module employs two kinds of interface connection, a 30-pin connector is used for the module electronics and two 12-pin connectors are used for the integral backlight system.

#### 3-2-1. LCD Module

- LCD Connector(CN1) : FI-X30SSL-HF (Manufactured by JAE) or Equivalent
- Mating Connector : FI-30C2L (Manufactured by JAE) or Equivalent

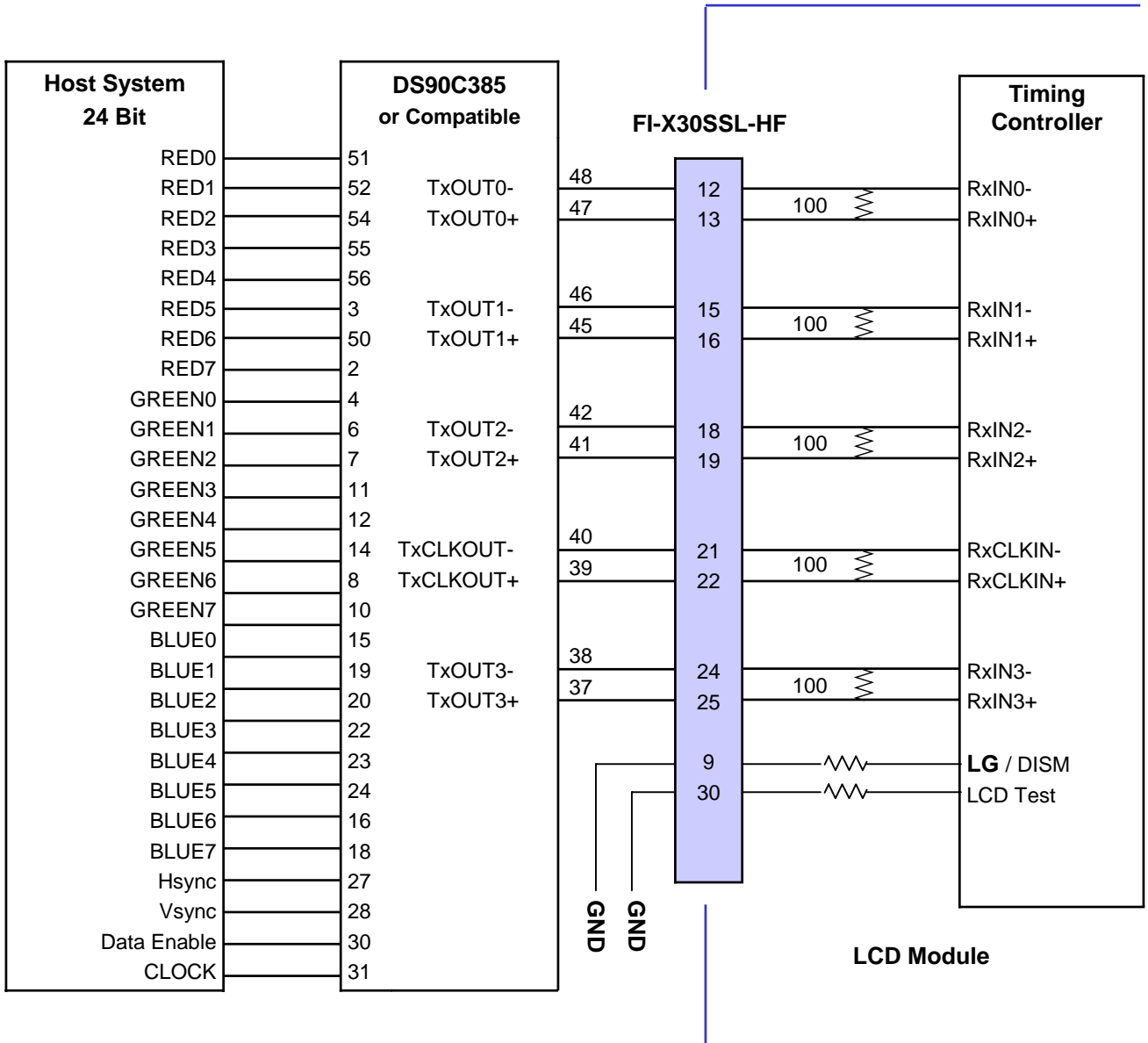
**Table 4. MODULE CONNECTOR(CN1) PIN CONFIGURATION**

Pin No.	Symbol	Description	Note
1	VLCD	Power Supply +12.0V	
2	VLCD	Power Supply +12.0V	
3	VLCD	Power Supply +12.0V	
4	VLCD	Power Supply +12.0V	
5	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	Select	Select LVDS Data format	1
10	DCR Enable	Dynamic CR Enable ( 'L' = Disable , 'H' = Enable )	2
11	GND	Ground	
12	RA-	LVDS Receiver Signal(-)	
13	RA+	LVDS Receiver Signal(+)	
14	GND	Ground	
15	RB-	LVDS Receiver Signal(-)	
16	RB+	LVDS Receiver Signal(+)	
17	GND	Ground	
18	RC-	LVDS Receiver Signal(-)	
19	RC+	LVDS Receiver Signal(+)	
20	GND	Ground	
21	RCLK-	LVDS Receiver Clock Signal(-)	
22	RCLK+	LVDS Receiver Clock Signal(+)	
23	GND	Ground	
24	RD-	LVDS Receiver Signal(-)	
25	RD+	LVDS Receiver Signal(+)	
26	GND	Ground	
27	VBR_OUT	VBR output form LCD module	
28	VBR_EXT	External VBR input from System to LCD module	
29	GND	Ground	
30	GND	Ground	3

- Note: 1. The pin no 9 is an option pin for DISM or LG format. ( LG Format = "GND" / DISM Format ="VCC")  
Please refer to page 9 and 10 for further details
2. The pin no 10 is an option pin for DCR Function ( Enable = "VCC" / Disable ="GND")
3. The pin no 30 is LCD Test option.  
LCM operates "AGP" (Auto Generation Pattern) or "NSB" (No Signal Black) is case that LVDS signals are out of frequency or abnormal condition in spite of 12 volt power supply.  
**LPL recommends "NSB"**. ( AGP : "VCC" or "OPEN" / NSB : "GND" )
4. All GND (ground) pins should be connected together, which should be also connected to the LCD module's metal frame.
5. All VLCD (power input) pins should be connected together.
6. Input Levels of LVDS signals are based on the IEA 664 Standard.

Product Specification

Table 5. REQUIRED SIGNAL ASSIGNMENT FOR LVDS TRANSMITTER ( Pin9="L" )

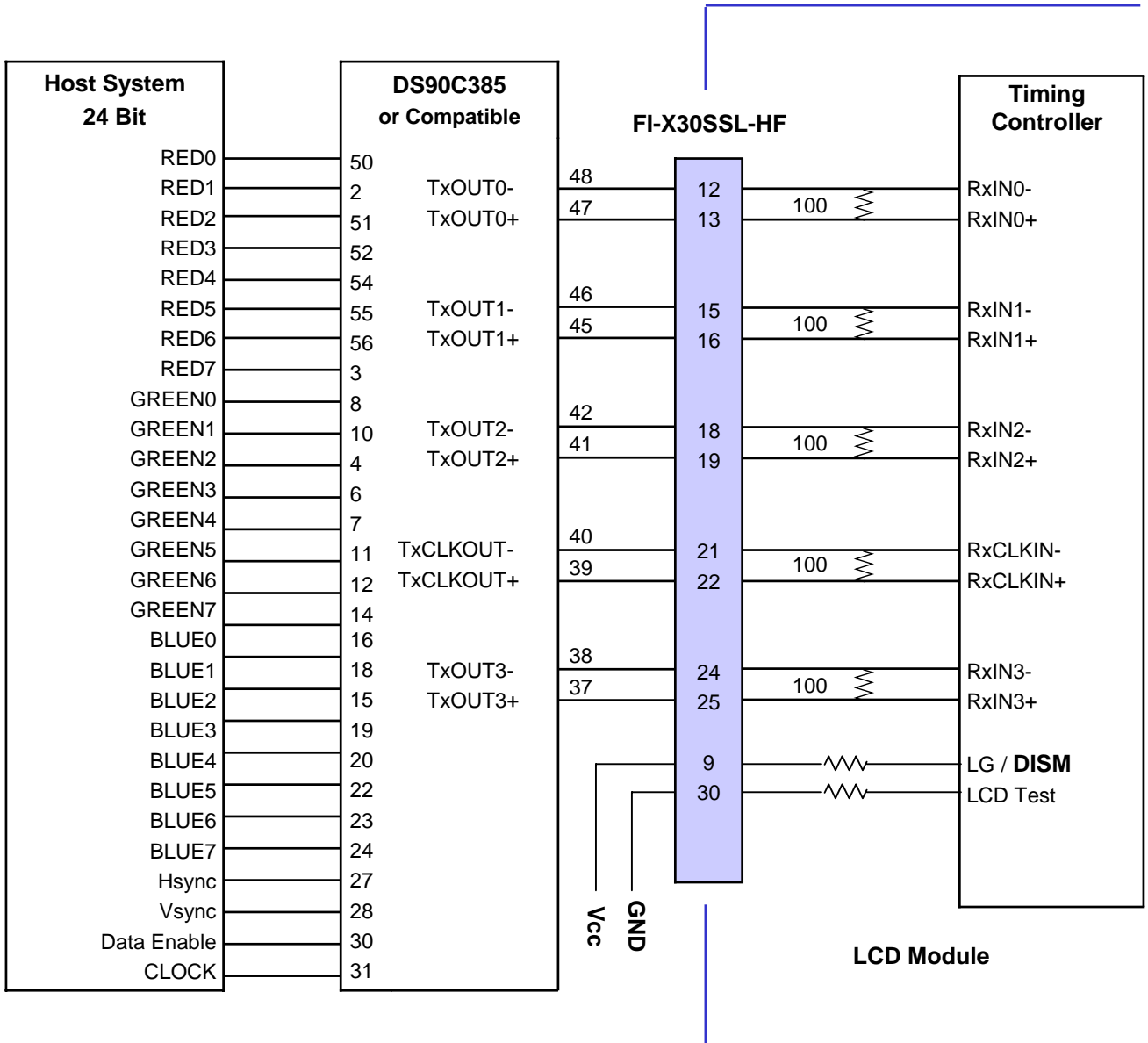


- Note: 1. The LCD Module uses a 100 Ohm[ ] resistor between positive and negative lines of each receiver input.  
 2. Refer to LVDS Transmitter Data Sheet for detail descriptions. (DS90C385 or Compatible)  
 3. '7' means MSB and '0' means LSB at R,G,B pixel data.



Product Specification

Table 6. REQUIRED SIGNAL ASSIGNMENT FOR LVDS TRANSMITTER ( Pin9="H" )



- Note: 1. The LCD module uses a 100 Ohm[ ] resistor between positive and negative lines of each receiver input.  
 2. Refer to LVDS Transmitter Data Sheet for detail descriptions. (DS90C385 or Compatible)  
 3. '7' means MSB and '0' means LSB at R,G,B pixel data.

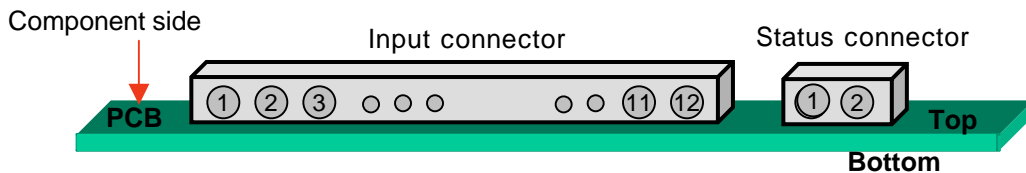
Product Specification

**3-2-2. Backlight Inverter**

- Inverter Connector : S12B-PH-SM3(manufactured by JST) or Equivalent
- Mating Connector : PHR-12 or Equivalent
- Status Connector
- Inverter Connector : 20022WR-02A00(manufactured by Yeon Ho co., Korea)
- Mating Connector : 20022HR-02S00(manufactured by Yeon Ho co., Korea)

**Table 7. INVERTER CONNECTOR PIN CONFIGURATION**

Pin No	Symbol	Description	Master	Slave	Note
1	VBL	Power Supply +24.0V	VBL	VBL	
2	VBL	Power Supply +24.0V	VBL	VBL	
3	VBL	Power Supply +24.0V	VBL	VBL	
4	VBL	Power Supply +24.0V	VBL	VBL	
5	VBL	Power Supply +24.0V	VBL	VBL	
6	GND	POWER GND	GND	GND	
7	GND	POWER GND	GND	GND	
8	GND	POWER GND	GND	GND	1
9	GND	POWER GND	GND	GND	
10	GND	POWER GND	GND	GND	
11	VBR	0V ~ 3.3V	VBR	Don't care	2
12	On/Off	0V ~ 5.0V	On/Off	Don't care	3
Option Pin(Lamp Open Status Detection)					
1	GND	POWER GND	GND		
2	Status	Upper 3.0V(Normal), Under 0.7V(Abnormal)	Status		



S12B-PH-SM3-TB  
(JST : Japan Solderless Terminal Co.,Ltd.)

Note : 1. GND should be connected to the LCD module's metal frame.

2. Minimum Brightness : VBR = 0.0V  
Maximum Brightness : VBR = 3.3V

3. VON : 4.0 ~ 5.0V  
VOFF : -0.3 ~ 0.5V

Product Specification

### 3-3. Signal Timing Specifications

Table 8 and Table9 show the signal timing required at the input of the LVDS transmitter. All of the interface signal timing should be satisfied with the following specification for normal operation.

**Table 8. TIMING TABLE for NTSC**

ITEM		SYMBOL	Min.	Typ.	Max.	Unit	Notes
DCLK Period		$t_{CLK}$	13.1	13.8	14.5	nsec	
DCLK Frequency		$f_{CLK}$	68.3	72.4	75.1	MHz	
Vertical	Frequency	$f_V$	57	60	63	Hz	
	Valid	$t_{VV}$	-	768	-	Line	
	Blank	$t_{VT} - t_{VV}$	8	22	295	Line	
	Total	$t_{VT}$	776	790	1063	Line	
Horizontal	Frequency	$f_H$	45	47.4	50	KHz	
	Valid	$t_{HV}$	-	1366	-	$t_{CLK}$	
	Blank	$t_{HT} - t_{HV}$	90	162	410	$t_{CLK}$	
	Total	$t_{HT}$	1456	1528	1776	$t_{CLK}$	

**Table 9. TIMING TABLE for PAL**

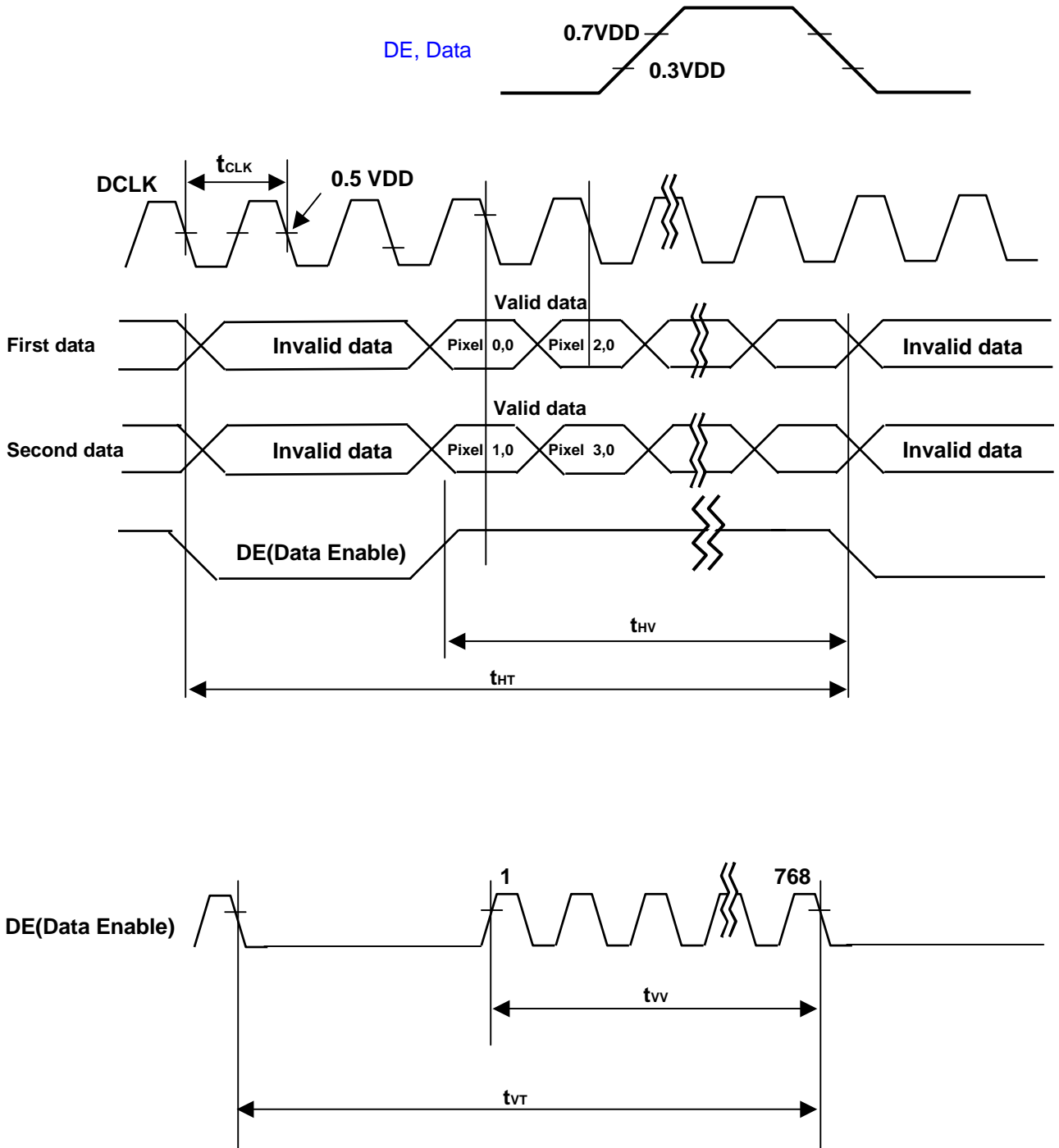
ITEM		SYMBOL	Min.	Typ.	Max.	Unit	Notes
DCLK Period		$t_{CLK}$	13.0	13.8	14.6	nsec	
DCLK Frequency		$f_{CLK}$	68.1	72.6	76.3	MHz	
Vertical	Frequency	$f_V$	47	50	53	Hz	
	Valid	$t_{VV}$	-	768	-	Line	
	Blank	$t_{VT} - t_{VV}$	8	182	295	Line	
	Total	$t_{VT}$	776	950	1063	Line	
Horizontal	Frequency	$f_H$	44.65	47.5	50.35	KHz	
	Valid	$t_{HV}$	-	1366	-	$t_{CLK}$	
	Blank	$t_{HT} - t_{HV}$	90	162	410	$t_{CLK}$	
	Total	$t_{HT}$	1456	1528	1776	$t_{CLK}$	

Note :

1. The performance of the electro-optical characteristics may be influenced by variance of the vertical refresh rate.
2. Above Timing Tables are only valid for DE Mode.

Product Specification

3-4. Signal Timing Waveforms



Product Specification

3-5. Color Data Reference

The brightness of each primary color(red,green,blue) is based on the 8-bit gray scale data input for the color. The higher binary input, the brighter the color. Table 10 provides a reference for color versus data input.

Table 10. COLOR DATA REFERENCE

Color		Input Color Data																							
		RED								GREEN								BLUE							
		MSB	LSB						MSB	LSB						MSB	LSB								
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (000) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (001)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	...	...								...								...							
	RED (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (000) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	...	...								...								...							
	GREEN (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BLUE	BLUE (000) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	...	...								...								...							
	BLUE (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Product Specification

3-6. Power Sequence

3-6-1. LCD Driving circuit

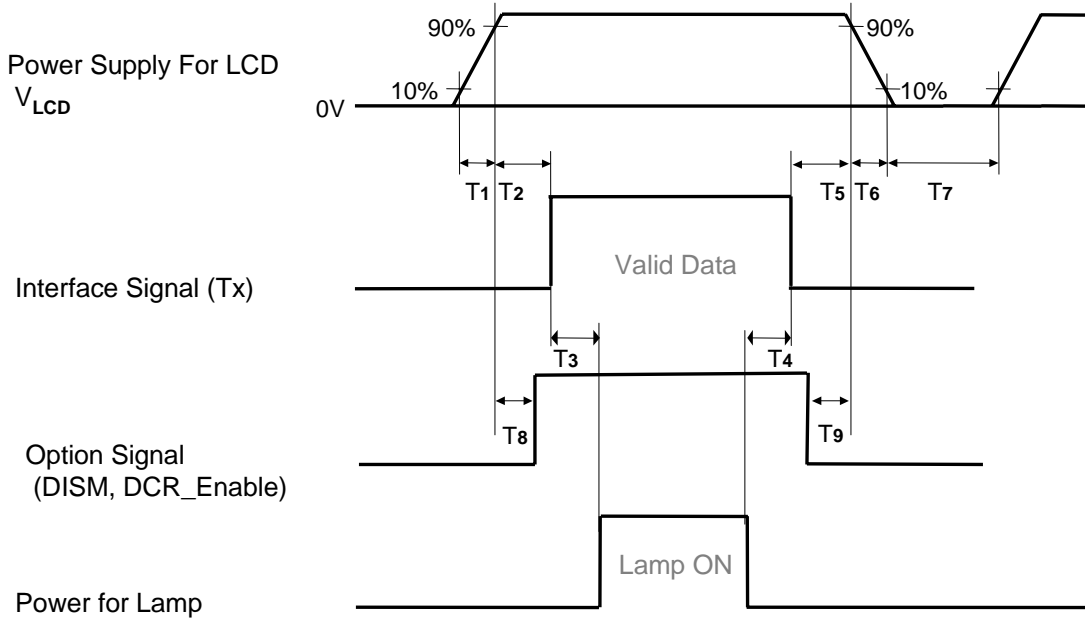


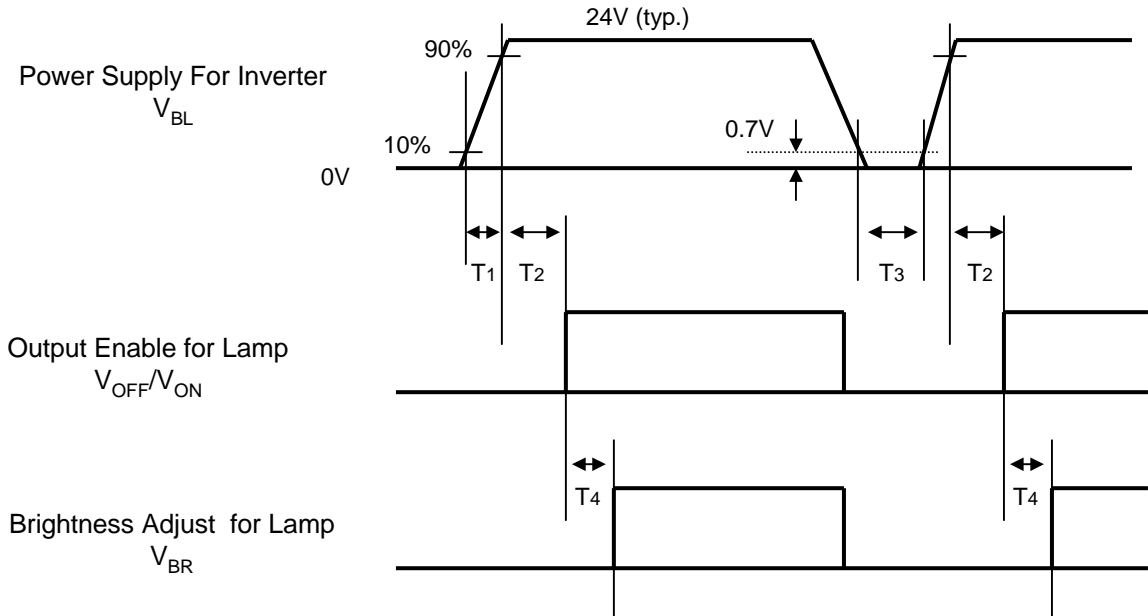
Table 11. POWER SEQUENCE

Parameter	Value			Unit
	Min	Typ	Max	
T1	1.0	-	20	ms
T2	5.0	-	50	ms
T3	200	-	-	ms
T4	200	-	-	ms
T5	0.5	-	50	ms
T6	-	-	300	ms
T7	1.0	-	-	s
T8	0 < T8 < T2			ms
T9	0 < T9 < T5			ms

- Note :
1. Please avoid floating state of interface signal at invalid period.
  2. When the interface signal is invalid, be sure to pull down the power supply  $V_{LCD}$  to 0V.
  3. The case when the T2/T5 exceed maximum specification, it operates protection pattern(Black pattern) till valid signal inputted. There is no reliability problem.
  4. The T3/T4 is recommended value, the case when failed to meet a minimum specification, abnormal display would be shown. There is no reliability problem.

Product Specification

3-6-2. ON/OFF for Inverter



3-6-3. Deep condition for Inverter

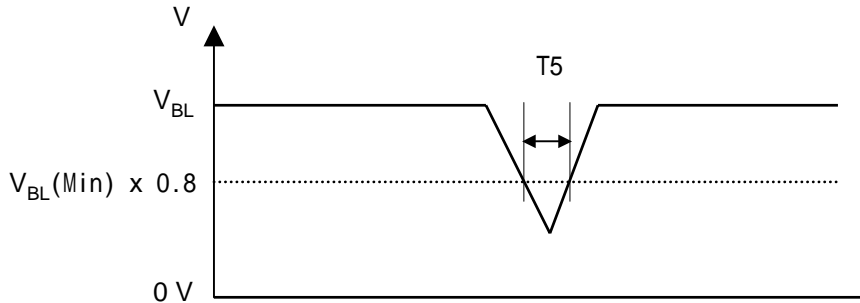


Table 12. POWER SEQUENCE FOR INVERTER

Parameter	Value			Unit	Remark
	Min	Typ	Max		
T1	20	-	-	ms	inverters connected condition
T2	500	-	-	ms	
T3	200	-	-	ms	
T4	0	-	-	ms	
T5	-	-	10	ms	$V_{BL}(\text{Min}) \times 0.8$

Product Specification

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at  $25 \pm 2^\circ\text{C}$ . The values are specified at an approximate distance 50cm from the LCD surface at a viewing angle of  $\Phi$  and  $\theta$  equal to  $0^\circ$ .

It is presented additional information concerning the measurement equipment and method in FIG. 1.

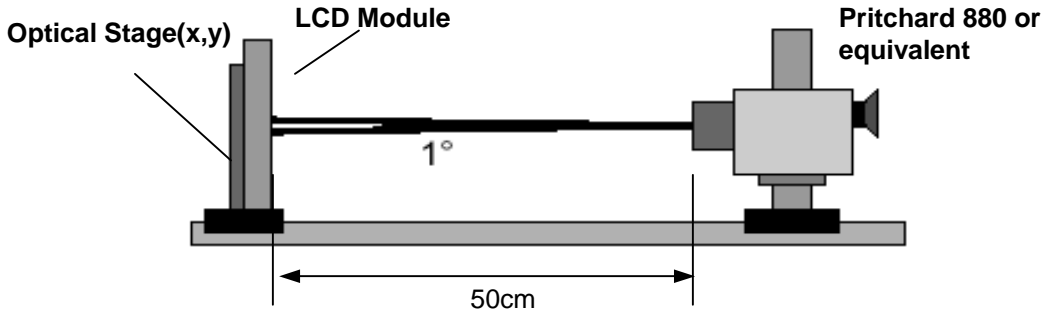


FIG. 1 Optical Characteristic Measurement Equipment and Method

Table 13. OPTICAL CHARACTERISTICS

$T_a = 25 \pm 2^\circ\text{C}$ ,  $V_{LCD} = 12.0\text{V}$ ,  $f_v = 60\text{Hz}$ ,  $D_{clk} = 72.4\text{MHz}$ ,  $V_{BR} = 3.3\text{V}$

Parameter	Symbol	Value			Unit	Note	
		Min	Typ	Max			
Contrast Ratio	CR	600	800			1	
	CR with DCR	1200	1600				
Surface Luminance, white	$L_{WH}$	400	500		$\text{cd/m}^2$	2	
Luminance Variation	$\delta_{WHITE}$ 5P			1.3		3	
Response Time (Gray to Gray)	Rise Time	$Tr_R$	-	8	12		
	Decay Time	$Tr_D$		10	14		
	G to G		-	8	12	ms	4
Color Coordinates [CIE1931]	RED	Rx	Typ -0.03	0.630	Typ +0.03		
		Ry		0.343			
	GREEN	Gx		0.275			
		Gy		0.607			
	BLUE	Bx		0.147			
		By		0.068			
	WHITE	Wx		0.281			
		Wy		0.293			
Viewing Angle (CR>10)							
	x axis, right( $\phi=0^\circ$ )	$\theta_r$	85	89	-	degree	5
	x axis, left ( $\phi=180^\circ$ )	$\theta_l$	85	89	-		
	y axis, up ( $\phi=90^\circ$ )	$\theta_u$	85	89	-		
	y axis, down ( $\phi=270^\circ$ )	$\theta_d$	85	89	-		
Gray Scale	Without DCR					6	
	With DCR						



Product Specification

Note :

1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

It is measured at center 1-point.

2. Surface luminance is the luminance value at center 1-point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see the FIG. 2.

3. The variation in surface luminance ,  $\delta$  WHITE is defined as :

$$\delta \text{ WHITE}(5P) = \text{Maximum}(L_{on1}, L_{on2}, L_{on3}, L_{on4}, L_{on5}) / \text{Minimum}(L_{on1}, L_{on2}, L_{on3}, L_{on4}, L_{on5})$$

Where  $L_{on1}$  to  $L_{on5}$  are the luminance with all pixels displaying white at 5 locations .

For more information, see the FIG. 2.

4. Response time is the time required for the display to transition from G(N) to G(M) (Rise Time,  $Tr_R$ ) and from G(M) to G(N) (Decay Time,  $Tr_D$ ). For additional information see the FIG. 3. ( $N < M$ )
5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 4.
6. Gray scale specification  
Gamma Value is approximately 2.2. For more information, see the Table 14.

**Table 14. GRAY SCALE SPECIFICATION**

Gray Level	Luminance [%] (Typ)	Luminance [%] (Typ) with DCR
L0	0.11	0.06
L15	0.19	0.16
L31	1.08	0.63
L47	2.07	1.68
L63	4.51	3.54
L79	7.75	6.41
L95	12.05	10.82
L111	17.06	16.74
L127	22.36	22.00
L143	28.21	27.44
L159	35.56	34.62
L175	43.96	42.94
L191	53.00	51.94
L207	63.37	62.25
L223	74.66	73.66
L239	88.17	87.05
L255	100	100

Product Specification

Measuring point for surface luminance & measuring point for luminance variation

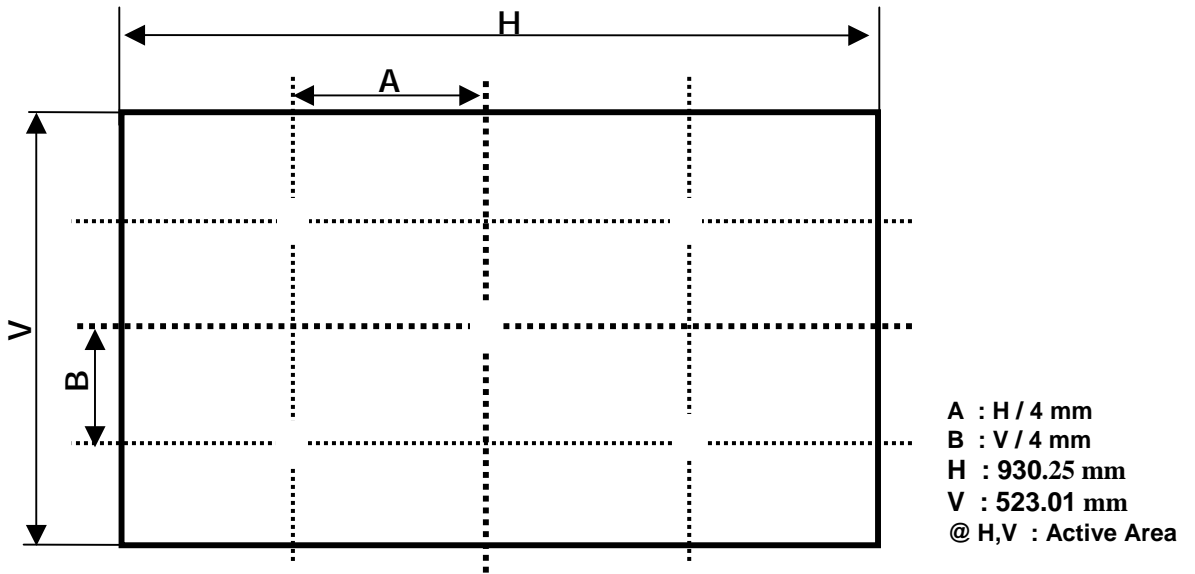


FIG.2 Measure Point for Luminance

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".

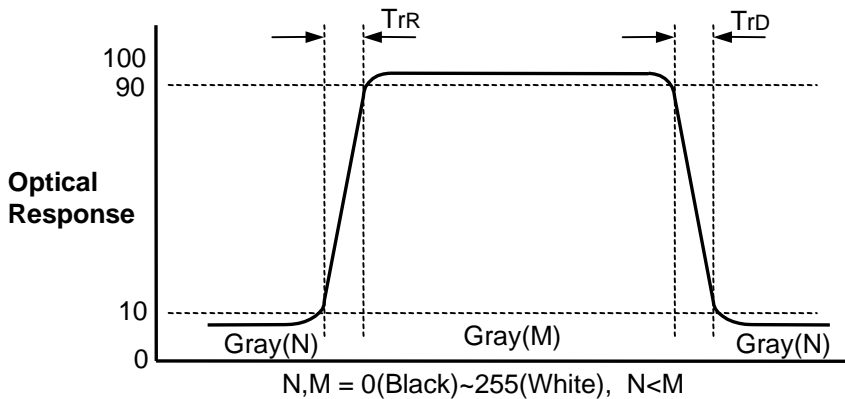


FIG.3 Response Time

Product Specification

Dimension of viewing angle range

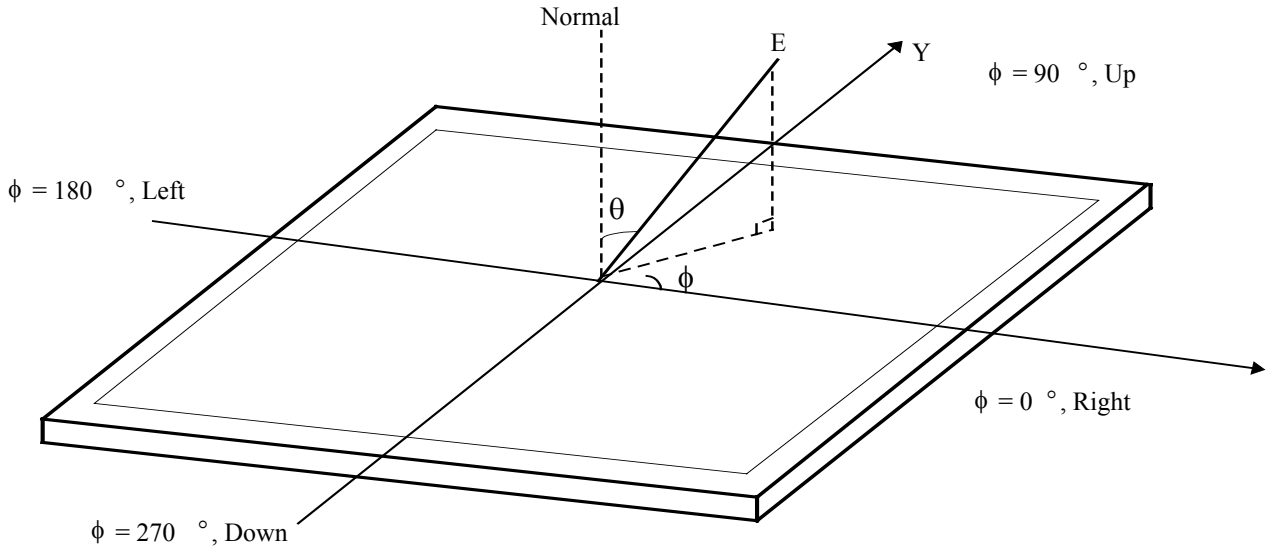


FIG.4 Viewing Angle

Product Specification

## 5. Mechanical Characteristics

The contents provide general mechanical characteristics. In addition the figures in the next page are detailed mechanical drawing of the LCD module.

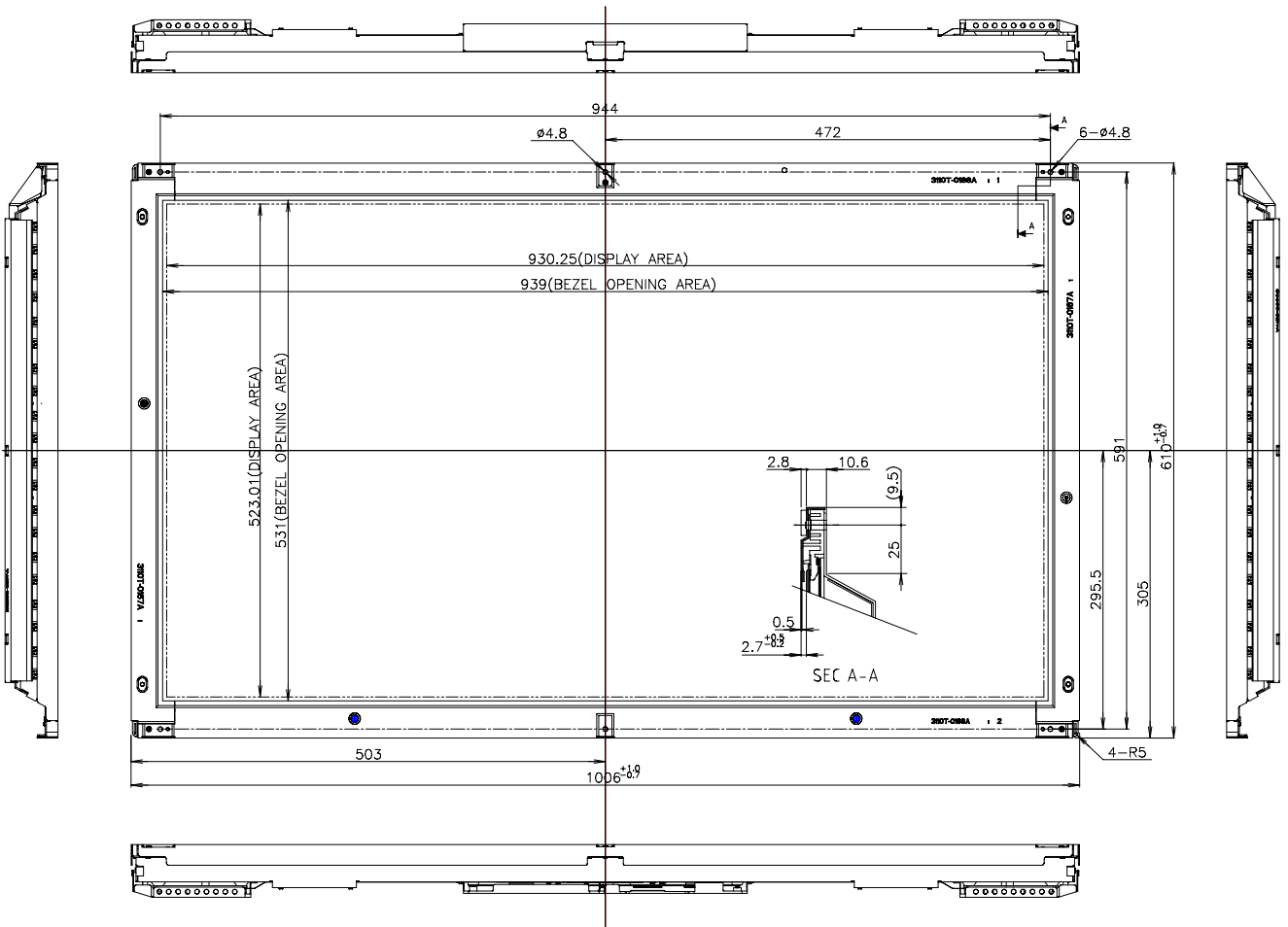
**Table 15. MECHANICAL CHARACTERISTICS**

Item	Value	
Outline Dimension	Horizontal	1006.0 mm
	Vertical	610.0 mm
	Depth	56.0 mm
Bezel Area	Horizontal	939.0 mm
	Vertical	531.0 mm
Active Display Area	Horizontal	930.25 mm
	Vertical	523.01 mm
Weight	14.5Kg (Typ.) , 15.5Kg (Max.)	
Surface Treatment	Hard coating(3H) Anti-glare treatment of the front polarizer	

Note : Please refer to page22 and 23 for mechanic drawings in terms of tolerance.

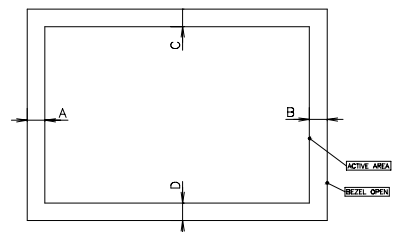
Product Specification

<FRONT VIEW>



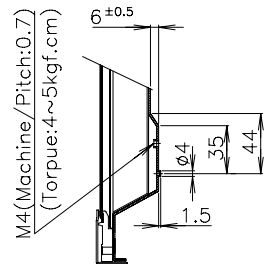
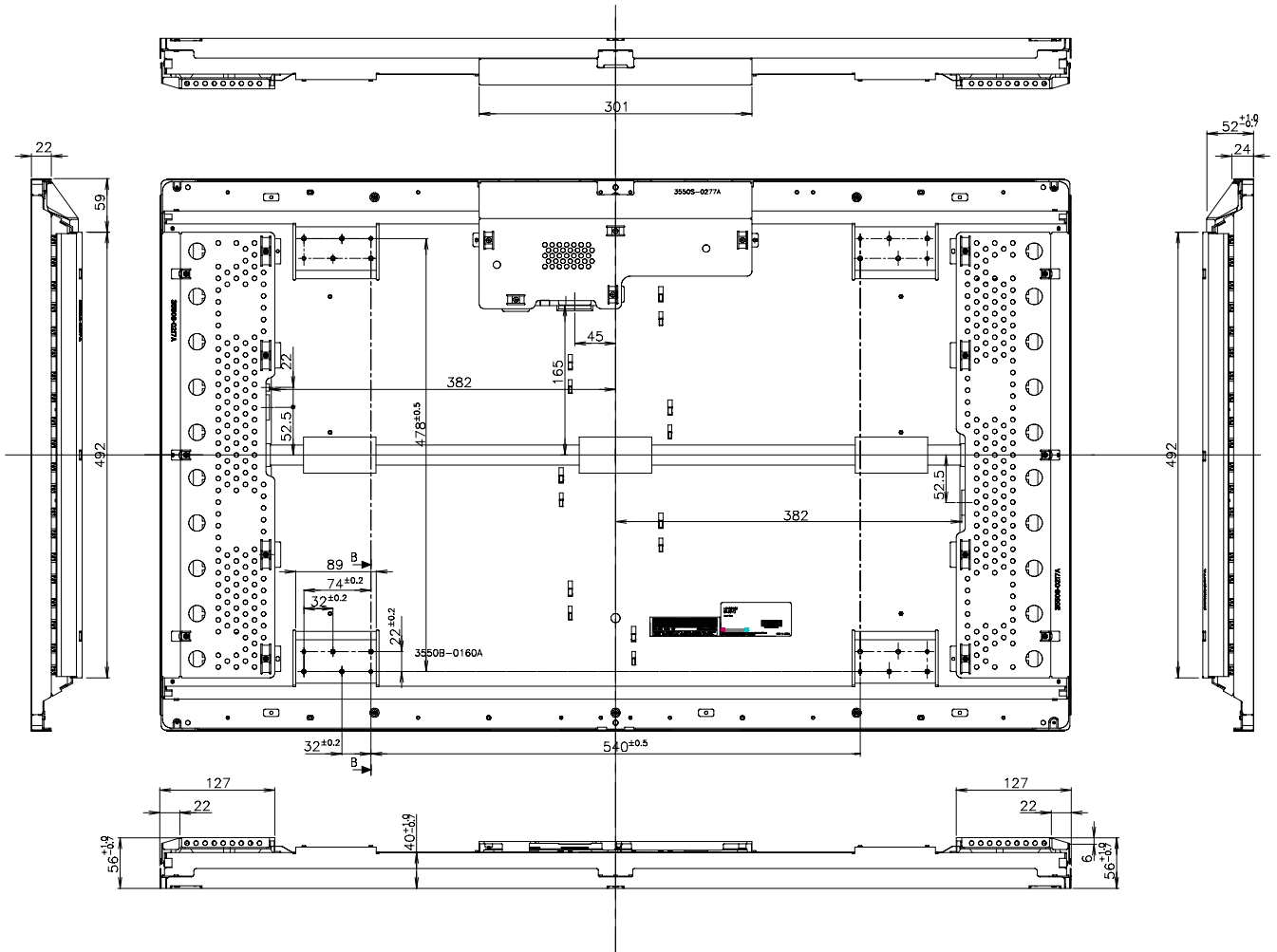
NOTE

1. UNSPECIFIED TOLERANCE IS  $\pm 1.0$ mm
2. GAP BETWEEN TOP CASE AND GLASS IS  $0.7^{+0.2}$
3. TILT AND A PARTIAL DISPOSITION TOLERANCE OF DISPLAY AREA ARE AS FOLLOW.
  - 1) X-DIRECTION :  $| A-B | \leq 1.5$ mm
  - 1) Y-DIRECTION :  $| C-D | \leq 1.5$ mm



Product Specification

<REAR VIEW>



SEC B-B

Product Specification

**6. Reliability**

**Table 16. ENVIRONMENT TEST CONDITION**

No.	Test Item	Condition
1	High temperature storage test	Ta= 50°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 40°C 50%RH 240h
4	Low temperature operation test	Ta= 0°C 240h
5	Vibration test (operating)	Wave form : random Vibration level : 1.0Grms Bandwidth : 10-300Hz Duration : X,Y,Z, 30 min One time each direction
6	Shock test (operating)	Shock level : 50Grms Waveform : half sine wave, 11ms Direction : ± X, ± Y, ± Z One time each direction
7	Humidity condition Operation	Ta= 40 °C ,90%RH
8	Altitude operating storage / shipment	0 - 14,000 feet(4267.2m) 0 - 40,000 feet(12192m)

## 7. International standards

### 7-1. Safety

- a) UL 60950-1:2003, First Edition, Underwriters Laboratories, Inc.,  
Standard for Safety of Information Technology Equipment.
- b) CAN/CSA C22.2, No. 60950-1-03 1<sup>st</sup> Ed. April 1, 2003, Canadian Standards Association,  
Standard for Safety of Information Technology Equipment.
- c) EN 60950-1: 2001, First Edition.  
European Committee for Electrotechnical Standardization(CENELEC)  
European Standard for Safety of Information Technology Equipment.

### 7-2. EMC

- a) ANSI C63.4 "Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHz to 40GHz. "American National Standards Institute(ANSI), 1992
- b) C.I.S.P.R "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment." International Special Committee on Radio Interference.
- c) EN 55022 "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment." European Committee for Electrotechnical Standardization.(CENELEC), 1998 ( Including A1: 2000 )

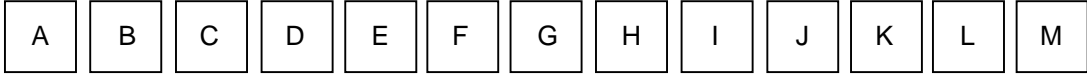


Product Specification

**8. Packing**

**8-1. Designation of Lot Mark**

a) Lot Mark



A,B,C : SIZE(INCH)  
E : MONTH

D : YEAR  
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial No. is printed on the label. The label is attached to the backside of the LCD module.  
This is subject to change without prior notice.

**8-2. Packing Form**

a) Package quantity in one box : 10 pcs

b) Box Size :1140 mm X 1000 mm X 810 mm.

## Product Specification

## 9. Precautions

Please pay attention to the followings when you use this TFT LCD module.

### 9-1. Mounting Precautions

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
- (7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.

### 9-2. Operating Precautions

- (1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :  
 $V = \pm 200\text{mV}$ (Over and under shoot voltage)
- (2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
- (3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)  
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
- (4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
- (7) Please do not give any mechanical and/or acoustical impact to LCM. Otherwise, LCM can't be operated its full characteristics perfectly.
- (8) A screw which is fastened up the steels should be a machine screw.  
(if not, it causes metallic foreign material and deal LCM a fatal blow)
- (9) Please do not set LCD module on its edge.

## Product Specification

### 9-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

### 9-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

### 9-5. Storage

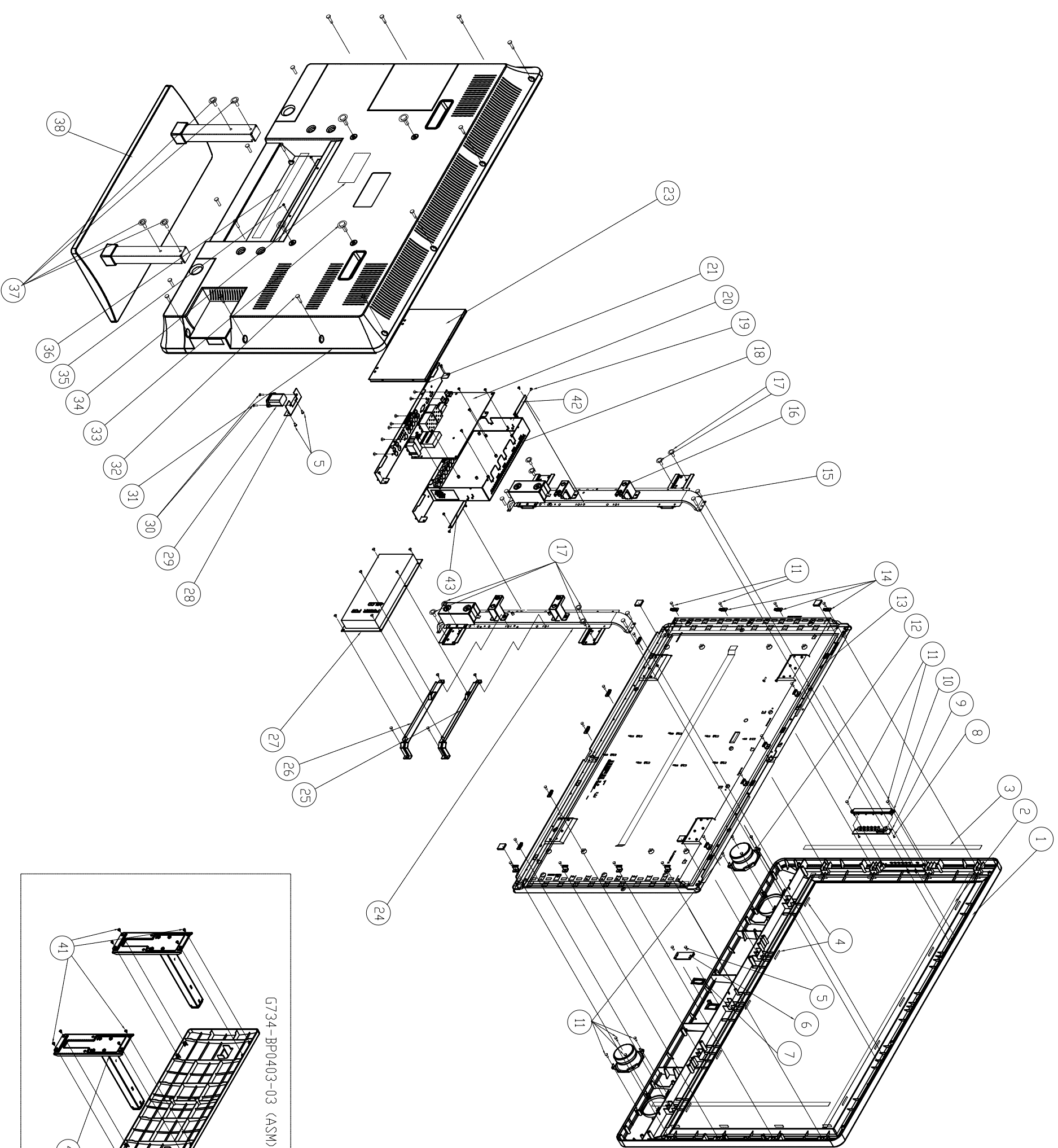
When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object.  
It is recommended that they be stored in the container in which they were shipped.

### 9-6. Handling Precautions for Protection Film

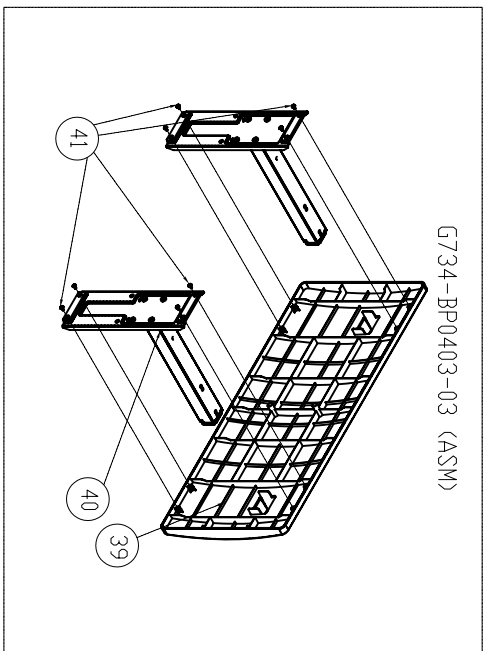
- (1) The protection film is attached to the bezel with a small masking tape.  
When the protection film is peeled off, static electricity is generated between the film and polarizer.  
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- (2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
- (3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

NOTE : THIS RELEASED DRAWING WAS PRODUCED BY COMPUTER , DO NOT UPDATE MASTER MANUALLY



G734-BP0403-03 (ASM)

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
45	G429-L42AC08-01SA	RHS SHIELD BOX BRACKET B RIGHT	4	
44	G429-L42AC08-01SA	RHS SHIELD BOX BRACKET A LEFT	8	
43	G429-L42AC08-01SA	RHS SHIELD BOX BRACKET A LEFT	8	
42	G429-L42AC08-01SA	RHS SHIELD BOX BRACKET A LEFT	8	
41	G712-BP0403-01A	RHS SHIELD BOX BRACKET A LEFT	8	ASM
40	G712-BP0403-01A	RHS SHIELD BOX BRACKET A LEFT	8	ASM
39	G231-BP0401-04ASA	RHS SHIELD BOX BRACKET A LEFT	1	ASM
38	G734-BP0403-03	RHS SHIELD BOX BRACKET A LEFT	1	ASM
37	G501-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
36	G578-L42AC08-02A	RHS SHIELD BOX BRACKET A LEFT	4	
35	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
34	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
33	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
32	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
31	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
30	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
29	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
28	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
27	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
26	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
25	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
24	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
23	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
22	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
21	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
20	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
19	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
18	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
17	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
16	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
15	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
14	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
13	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
12	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
11	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
10	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
9	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
8	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
7	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
6	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
5	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
4	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
3	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
2	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	
1	G502-309015-00	RHS SHIELD BOX BRACKET A LEFT	4	



DRAWN.	CHECKED	APPRD.	3rd ANGLE PROJECTION	TOLERANCE UNLESS OTHERWISE SPECIFIED 9-MM-8 MM ±0.1 8-MM-25MM ±0.15 25MM-80MM ±0.2 80MM-250MM ±0.3 250MM-ABOVE ±0.6	ANGULAR: ±1°	FINISH	SCALE NIL
				KAWA ELECTRONIC R & D CENTRE		TITLE: GLCT42AEAIAPS-B01	
				MATERIAL		MODEL NO. LCT42AE	
				PART NO. GLCT42AEAIAPS-B01		DWG. NO. L42AEEXPA	
				QTY.		SHEET 1 OF 1	

DWG. REV. ZONE	DESCRIPTION	DATE	REVISOR

## Spare part list for LCT42Z5TAP

Item	Part Number	Part Description	Usage / unit	Unit	Key/Spare
1>	GLCT42AEAIA1PS-B01	ROHS AKAI LCT42AE (LCT42Z5TAP) S-MT5371 LPL (LC420W02-SLA1 V1.0) AC120V/60HZ USA BLACK/ SILVER HORIZONTAL ATV/DTV			
	G510-L42AE02-04AKA	ROHS HORIZONTAL CARTON BOX AKAI LCT42Z5TAP S- MT5371 LPL USA K ZHEN XING	1.000000	Piece	K
2>	G580-K00201-01CPA	ROHS IB E FOR AKAI W/O DVD K002(OMNIPOTENCE) REMOTE CONTROL USA ADD SAFETY (CHENG YI)	1.000000	Piece	K
3>	G580-L42AE2D-01APA	ROHS IB E FOR LCT42Z5TAP AKAI TV+ATSC NO PIP LPL MT5371 USA(CHENG YI)	1.000000	Piece	K
4>	GE7501-063009-1A	ROHS REMOTE CONTROC K002 231 MASK "AKAI"64KEYS BLACK (COMMON) OMNIPOTENCE (CHUAN QI SHENG)	1.000000	SET	K
5>	GE7801-P02004-1	ROHS PCB ASSY PSU BOARD MEGMEET MLT198K FOR 42LCD AC110-240V OUTPUT 5V/9V/12V/24V 300W	1.000000	SET	K
6>	G771EL37AD06-02	ROHS MAIN PCB ASS'Y S- MT5371 LPL USA	1.000000	SET	K
7>	G200-L42AE12-05AAA	ROHS CABINET FRONT MATT BLACK/SILVER LCT42Z5TAP S- MT5371 LPL USA P	1.000000	Piece	S
8>	G202-L42AE01-01AAA	ROHS CABINET BACK BLACK W/ O DVD/POWER SWITCH LCT42AE A(AKAI PLASTIC)	1.000000	Piece	S
9>	G269-42SD01-01LA	ROHS REMOTE RECEIVE LENS (AKAI PLASTIC)	1.000000	Piece	S
10>	G300-L42AE13-02CA	ROHS POLYFOAM BOTTOM EPS (SHANG HAO)	1.000000	Piece	S
11>	G300-L42AE14-02CA	ROHS POLYFOAM TOP EPS (SHANG HAO)	1.000000	Piece	S
12>	G310-041204-01VA	ROHS POLYBAG 4"X12"X0.04 AV (AO LANG)	1.000000	Piece	S
13>	G310-111404-07VA	ROHS POLYBAG 11"X14"X0.04 FV (AO LANG)	1.000000	Piece	S
14>	G310-504004-01A	ROHS POLYBAG EPF 50"X40"X0.04 ao LANG	1.000000	Piece	S
15>	G370-42D102-01A	ROHS PAD CORD SPONG FOR SPK (ZHI QIANG SHENG)	1.000000	Piece	S
16>	G370-L42AE01-01A	ROHS SUPPORT CUSHION 18X18X4MM(ZHI QIANG SHENG)	4.000000	Piece	S

## Spare part list for LCT42Z5TAP



17>	G389-L42AE01-01A	ROHS PVC SHEET 30X5X1.0MM WITH ADHESIVE BLACK JIA LI	8.000000	Piece	S
18>	G426-L37AD02-01SA	ROHS AC JACK BRACKET (TOMEI)	1.000000	Piece	S
19>	G429-L42AE0B-01SA	ROHS SHIELD BOX BRACKET B RIGHT(TOMEI)	1.000000	Piece	S
20>	G436-L42AE09-01SA	ROHS TERMINAL SHEET FOR 5371 HDMIX2(TOMEI)	1.000000	Piece	S
21>	G483-L42AE11-01A	ROHS SHIELD BOX L42AE (TOMEI)	1.000000	Piece	S
22>	G521-030091-01A	ROHS FELT PAPER 30X9X1.0MM W/ADHESIVE(ZHI QIANG SHENG)	10.000000	Piece	S
23>	G521-550155-01A	ROHS FELT PAPER 550X15X0.5MM W/ADHESIVE (ZHI QIANG SHENG)	2.000000	Piece	S
24>	G521-950155-01A	ROHS FELT PAPER 950X15X0.5MM W/ADHESIVE (ZHI QIANG SHENG)	2.000000	Piece	S
25>	G522-421D01-01A	ROHS MASKING PAPER (ZHI QIANG SHENG)	1.000000	Piece	S
26>	G560-L42AE01-05APA	ROHS MODEL LABEL AKAI LCT42Z5TAP S-MT5371 LPL USA P(QIAN SE)	1.000000	Piece	S
27>	G563-119-A	ROHS SERIAL NO. LABEL	1.000000	Piece	S
28>	G568-P46T02-02A	ROHS WARNING LB ENG 42SF NIL	1.000000	Piece	S
29>	G578-L42AD01-02APA	ROHS FUNCTION SHEET FOR TERMINAL L42AD(S-MT5371) HDMIX2 USA ENG P(QIAN SE)	1.000000	Piece	S
30>	G579-42D102-09A	ROHS SERIAL NO/BAR CODE LABEL 42D1	1.000000	Piece	S
31>	G579-42D105-01A	ROHS PROTECTIVE EARTH LABEL FOR ESA 42TD1	1.000000	Piece	S
32>	G579-L27AD09-01A	ROHS CAUTION LABEL ENG AKAI (QIAN SE)	1.000000	Piece	S
33>	G579-L32AD09-02APA	ROHS FCC STATEMENT LABEL 77X20MM(QIAN SE)	1.000000	Piece	S
34>	G579-L42AE01-05APA	ROHS BAR CODE LABEL AKAI LCT42Z5TAP W/SERIAL NO.USA P(QIAN SE)	2.000000	Piece	S
35>	G579-L42AE04-02APA	ROHS POP LABEL AKAI LCT42Z5TAP USA P(QIAN SE)	1.000000	Piece	S

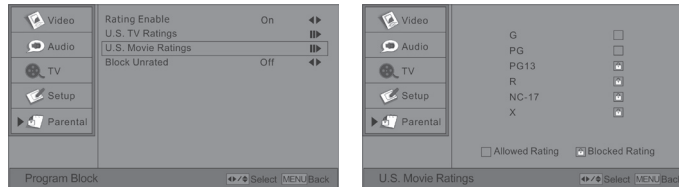
## Spare part list for LCT42Z5TAP

36>	G590-L42AE01-04APA	ROHS WARRANTY CARD AKAI ENG LCT42Z5TAP USA P(QIAN SE)	1.000000	Piece	S
37>	G593-L42AE01-04APA	ROHS QUICK START GUIDE AKAI ENG LCT42Z5TAP USA P (QIAN SE)	1.000000	Piece	S
38>	G599-BP0401-01APA	ROHS IB SHEET E FOR LCT42AE STAND(SAME AS 599- L42AE01-01BP) USA(QIAN SE)	1.000000	Piece	S
39>	GE3404-157004A	ROHS AC CORD UL 1.88M (YY-3/ ST3 YUNBIAO) (YUN HUAN)	1.000000	Piece	S
40>	GE3421-925153A	ROHS WIRE ASSY 250MM 3WIRES 20# 1617 FOR POWER IN PUT (YUN HUAN)	1.000000	Piece	S
41>	GE3421-925241A	ROHS WIRE ASSY 1H2.5-2H2.5 L=480 AG 12+8 LCT37" MT5371 (HU GUANG)	1.000000	Piece	S
42>	GE3461-000132A	ROHS WIRE ASSY 1H2.0- 2H2.5/2.0 L800/600 AG 12/10+4P LPL 42" S02 INVERTER (HU GUANG)	1.000000	Piece	S
43>	GE3461-000141A	ROHS WIRE ASSY 1H2.0-2H2.5 L350 AG 12/10P LCD42" LPL INVERTER (HU GUANG)	1.000000	Piece	S
44>	GE3471-000090A	WIRE WS SHIELD WIRE LCT422D L=300MM LPL MT8202 LVDS (HU GUANG)	1.000000	Piece	S
45>	GE3471-000103A	ROHS WIRE WS 1H2.0-2H2.0 L=550 DI 13P/6+8P LCT27&42" MT5371 KEY (HU GUANG)	1.000000	Piece	S
46>	GE4801-136001A	ROHS SPEAKER 6 OHM 12W D3" (JUN LANG)	2.000000	Piece	S
47>	GE6203-42PD02	ROHS DISPLAY LCD 42" LPL WXGA TFT LC420W02-SLA1	1.000000	Piece	S
48>	GE7301-010002A	ROHS BATTERY AAA R03P1.5V <2> (CHAO YANG)	2.000000	Piece	S
49>	G734-BP0403-03	ROHS PLASTIC STAND FOR 421D CD=460MM W/PACKING EXPLODE H=270MM MATT BLACK (P320-605871K-00)	1.000000	SET	S
50>	G771BL26AE01-01	ROHS IR RECEIVE PCB ASS'Y S- MT5370+DVD CMO	1.000000	SET	S
51>	G771KL42AE04-01	ROHS KEY (MAIN 7KEY) PCB ASS'Y S-MT5371 LPL	1.000000	SET	S

## If you forget your V-Chip Password:

### ◆ Using the “U.S. Movie Ratings” item

- 1 After entering the “Program Block” menu, press ▲ or ▼ button to highlight the “U.S. Movie Ratings” item.
- 2 Press ► or **Enter** button to enter.
- 3 Press ▲ or ▼ button to select an item, then press the **Enter** button to lock (display “”) or unlock (display “”).



### For Movie previously shown in theaters:

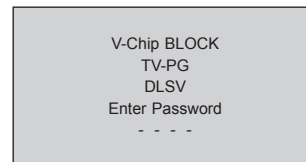
- G (general audience)
- PG (parental guidance suggested)
- PG-13 (13 years and older)
- R (Restricted)
- NC-17 (18 years and older)
- X (Adult)

If you set PG-13: G and PG movies be available, PG-13, R, NC-17, and X will be blocked.

- 4 Press the **Menu** button to exit the sub-menu.

### ● Unlocking programs temporarily

- 1 If you try to watch a program that exceeds the TV Guideline you set, the system enters program lock mode. You can either unlock the program temporarily or select a non-locked program to watch.
- 2 To temporarily unlock the program, press the Number buttons (0~9) to enter your 4-digit password.



If the correct code is entered, the program lock mode is released and the normal picture appears.



# Software Upgrade

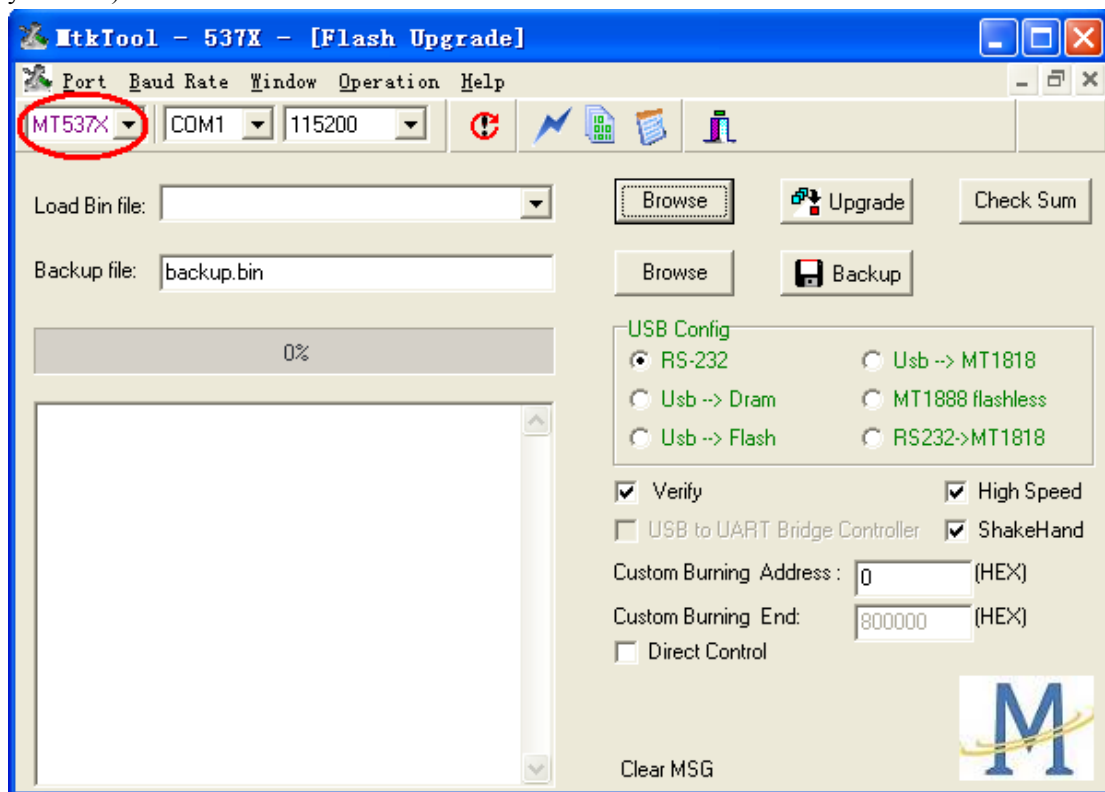
## Process of update MT537X

### Preparing :

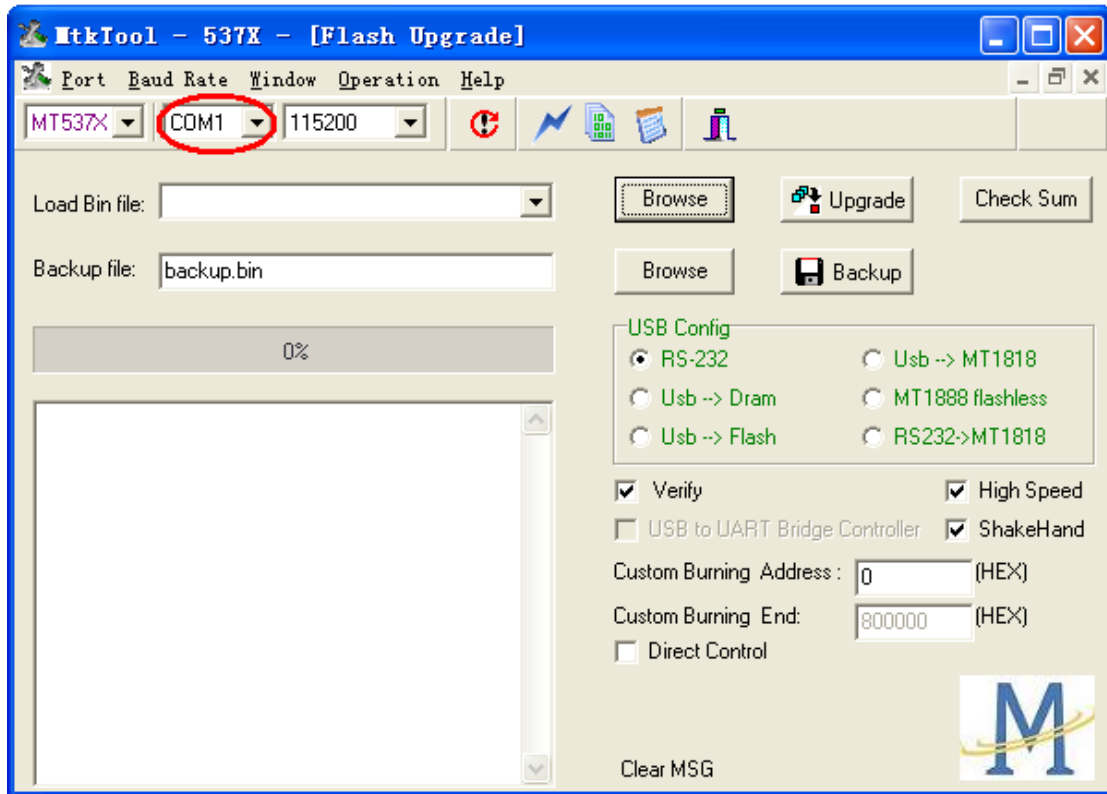
1. Connect the Plasma/LCD TV and PC with the **Software Upgrade Board**. Please find the details for connecting **referring to the appendix at the end of this file**.
2. Store the MtkTool into the PC .

### Downloading :

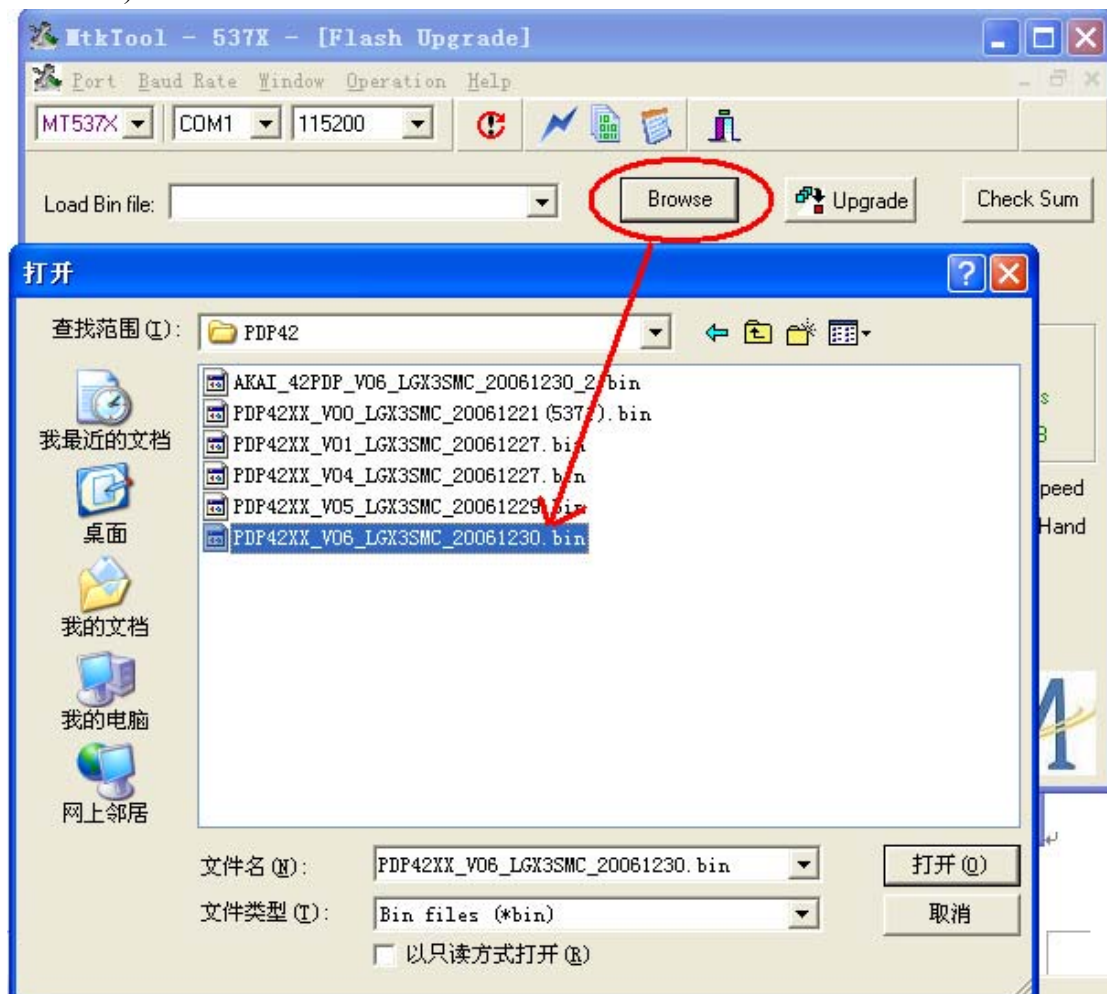
3. Turn on AC power of the TV and then press the button “standby” of the remote control . The image could be found on the screen of the TV while the color of the power indicator is green .
4. Execute MTKtool and select the chipset as MT537X. (the software of MTKtool will be sent to your side)



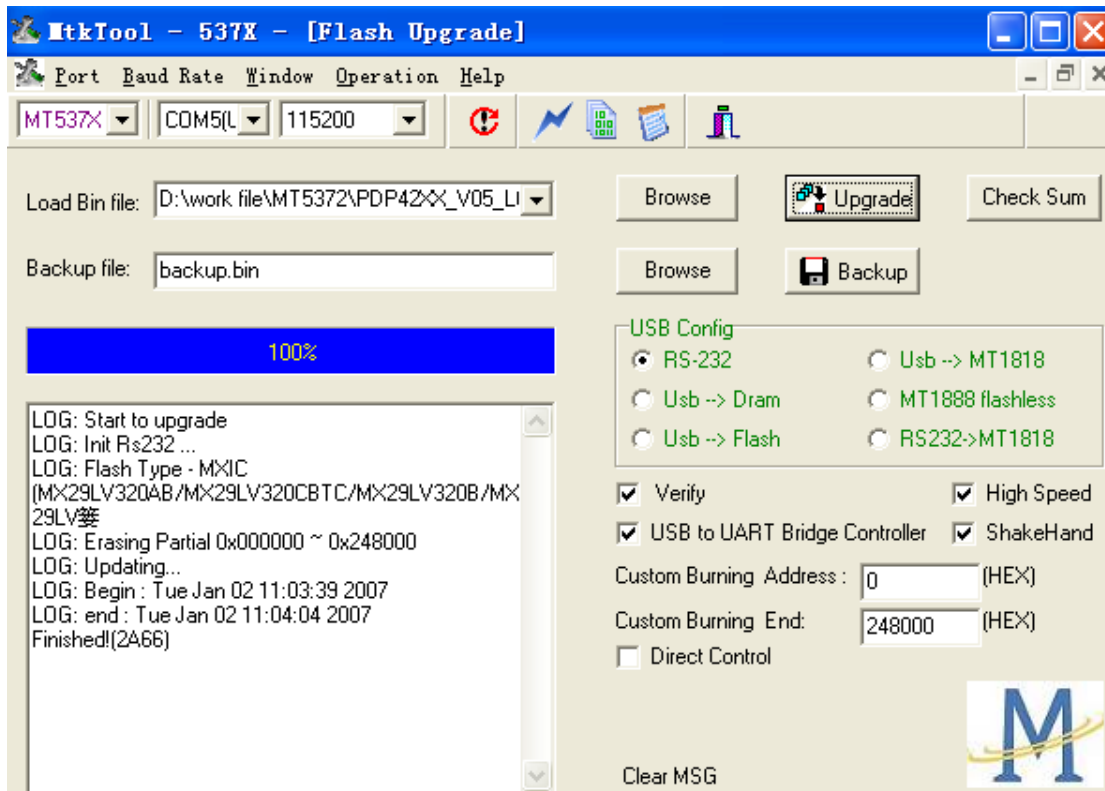
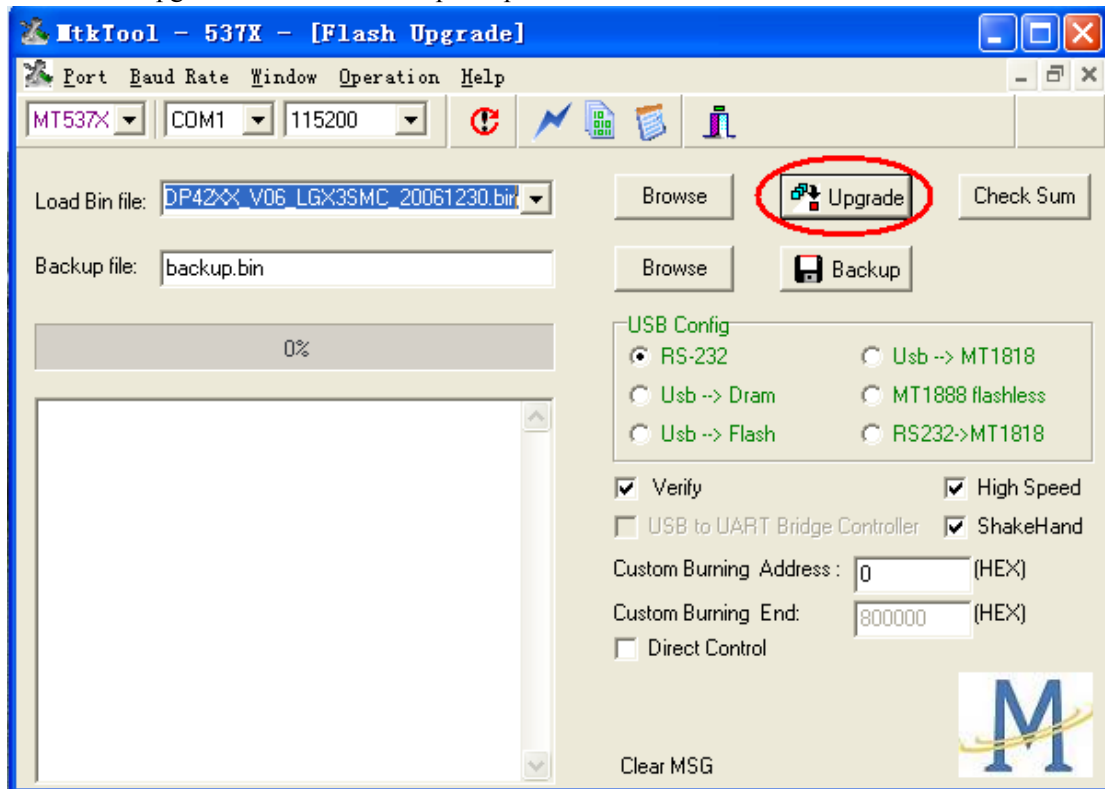
5. Select current COM port. (please try to check the COM port of your PC).



6. Choose the bit rate as 115200.
7. Select the update binary by pressing browse button. For example, the binary file name is PDP42XX\_V06\_LGX3SMC\_20061230.bin. (this update firmware will be sent to your side)



- Press Upgrade button and start update process.



- The update process is successful as the progress bar is 100%. After the update process is ok, turn off power and wait indicator light is off. Turn on power and TV can work.

## Checking

It is needed to check the version of the firmware for MT5371 which has been download into the TV .

Press Menu button of the remote control, following input “5371” of the remote control and OSD menu for Factory Setting is appeared on the screen .

Use the remote control and select the item of “Version Info” and then press “Enter” button of the remote control. It is easy to be found the version of the current firmware for MT5371 is as the following : “Model Name : PDP42Z5TA / Version:V17\_LGX3SMC\_20070119 ”

## **Appendix:**

### **Quick Installation Guide**

**For**

### **Software Upgrade Board**

#### **1. Parts List**

- Software upgrade board x 1 (#1)
- RS232 null cable x 1 for PC (#2)
- RS232 – VGA cable (#4)
- USB cable x 1 (#5)

#### **2. Installation for ATV upgrade**

##### **2.1 Connect RS232 cable (#2) to PC serial port**



**Connect another side of RS232 cable (#2) to the board (#1)**



**2.2 Connect RS232-VGA cable (#4) (RS232 side) to the board (#1)**



**Connect RS232-VGA cable (#4) (VGA side) to the TV**



**2.3 Connect USB cable (#5) to the board (#1)**

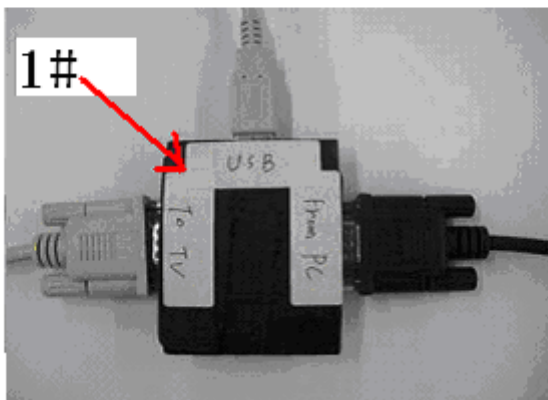


**Connect another side of USB cable (#5) to PC**

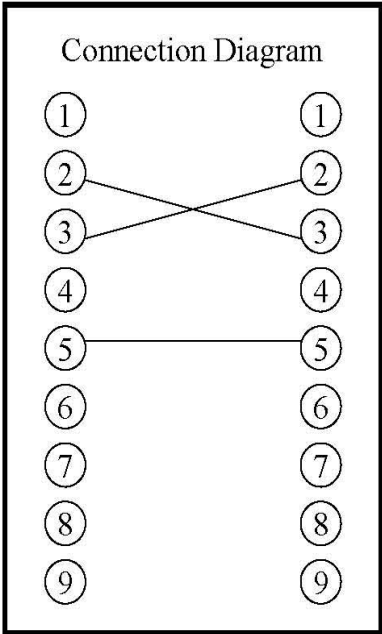
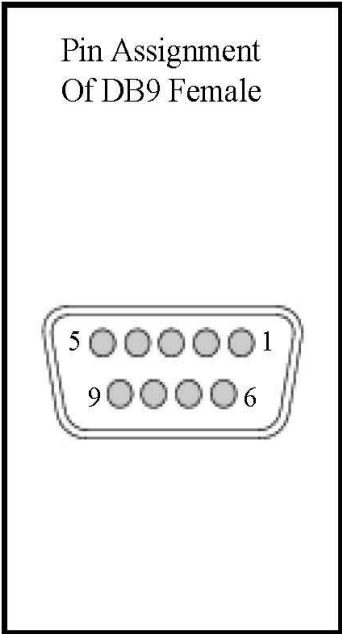
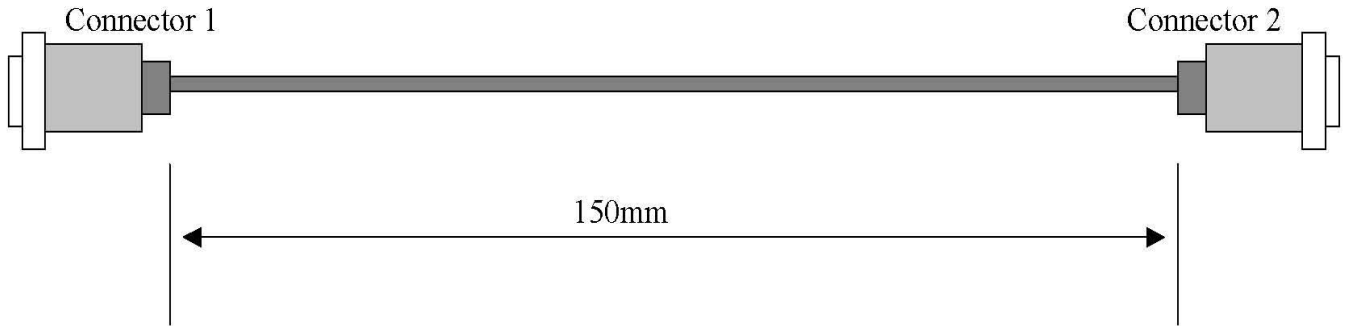


### 3. Cables Standard for Upgrade Board

**Software upgrade board x 1 (#1)**

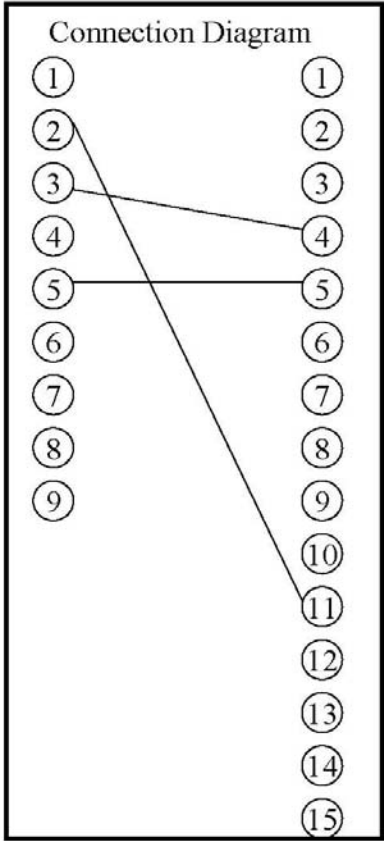
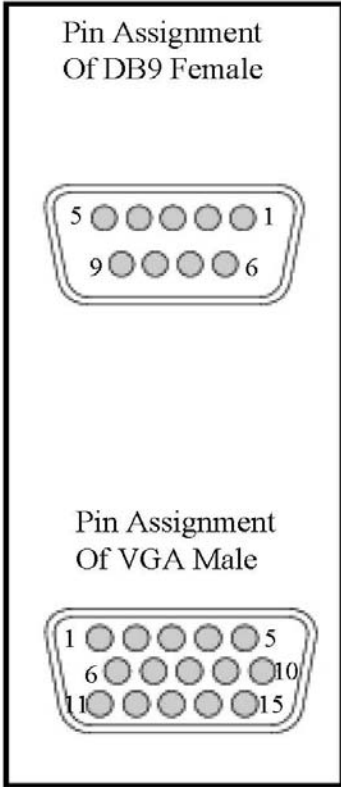
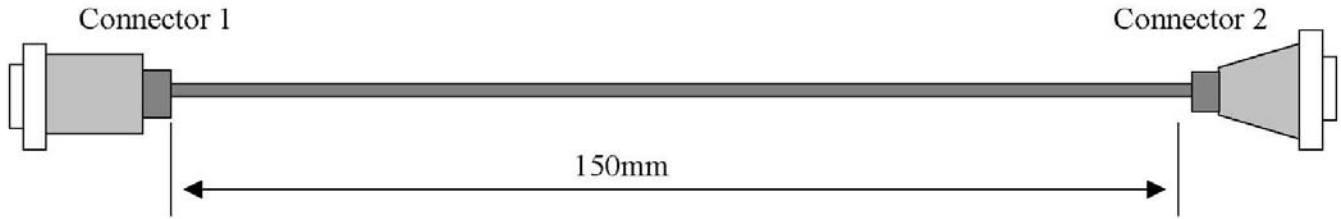


# RS232 Null Cable for PC (#2)



Connector 1: DB9 Female  
Connector 2: DB9 Female

# RS232 - VGA Cable (#4)

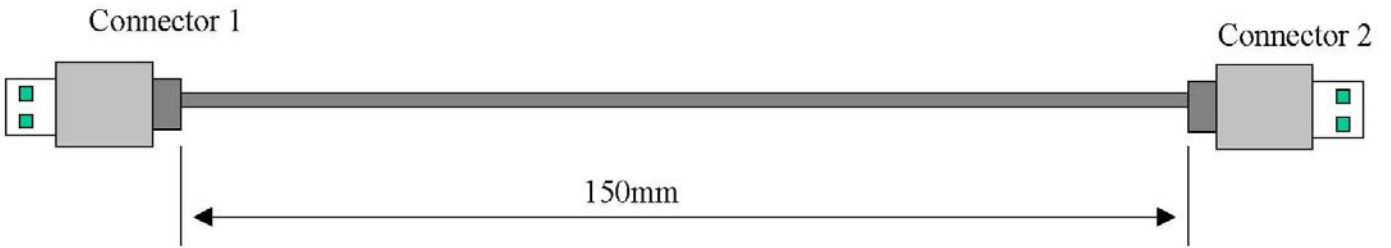


Connector 1: DB9 Female  
Connector 2: VGA Male



# USB Cable (#5)

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Connector 1: Standard USB Male  
Connector 2: Standard USB Male